European Commission

FVLLMONTI

Call: **H2020-FETPROACT-2020-01**

Grant Agreement no. **101016776**

Deliverable D2.3

Parasitic Element Extraction

Start date of the project: 1st February 2021

FVLLMONTI

Duration: 60 months
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DOCUMENT CLASSIFICATION

Title	**Parasitic element extraction**
Deliverable	**D2.3**
Estimated Delivery	28/02/2023 (M26)
Date of Delivery Foreseen	28/02/2023
Actual Date of Delivery	28/02/2023
Authors	Chhandak Mukherjee – P1 – UBx Marina Deng – P1 – UBx Bruno Neckel Wesling –P1 – UBx Cristell Maneux – P1 – UBx
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Work package	WP2
Dissemination	CO (Confidential)
Version	V1.2
Doc ID Code	D2.3_FVLLMONTI_P1-MUKHERJEE-230222
Keywords	VNWFET, junctionless (JL), vertical nanowire (VNW), device, S-parameters, interconnect parasitic, Electro-magnetic (EM) simulation, On-wafer measurement, de-embedding, electrical equivalent circuit.

DOCUMENT HISTORY

Version	Date	Modification
1.0	30/01/2023	First version
1.1	13/02/2023	Intermediate revision
1.2	28/02/2023	Final version

DOCUMENT ABSTRACT

This document describes an elaborate methodology for the extraction of the extrinsic parasitic interconnects of the FVLLMONTI technology: the elementary JunctionLess (JL) Vertical NanoWires Field-Effect Transistor (VNWFET). These devices are fabricated at LAAS-CNRS in WP1 (Fabrication of VNWFET technologies from devices to logic blocks) for the purpose of parameter extraction in WP2 and to provide necessary inputs for WP3 (TCAD and compact modelling).

The methodology developed for the T2.2 of this WP relies on the accurate reconstruction of the small-signal electrical equivalent circuit of parasitic elements extrinsic to the VNWFETs. Specifically, the parasitic network is represented by interconnects and the pads of the RF test structures for the 3D VNWFET technology. The methodology is based on the extraction of the distributed parasitic elements from an open test-structure, for which on-wafer S-parameter measurements were carried out up to 40 and 110 GHz. The electrical equivalent circuit of the passive device was then constructed and used for de-embedding of the transistor S-parameters for extraction of intrinsic small-signal parameters such as the gate capacitances. This extraction step is particularly important for the FVLLMONTI value chain in order to ensure an accurate compact modeling of the dynamic behavior of the intrinsic VNWFETs and subsequent logic circuit design simulations.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101016776.

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LIST OF ACRONYMS / GLOSSARY

D: Deliverable
M: Month of the project
L: Lead
P: Partner
PU: Public
V: Version
WP: Work Package
VNWFET: Vertical Nanowire Field Effect Transistor
JL: JunctionLess
VN: Vertical Nanowire
GAA: Gate All-Around
RF: Radio-Frequency
DUT: Device under Test
SOLT: Short-Open-Load-Thru
GSG: Ground-signal-ground
VNA: Vector Network Analyzer
PNA: Programmable Network Analyzer
ADS: Advance Design System
GDSII: Graphic Design System (stream format II)
SSEC: Small Signal Equivalent Circuit
EM: Electro-Magnetic
TCAD: Technology Computer-Aided Design
EDP: Energy-Delay Product
PDP: Power-Delay Product
DTCO: Design-Technology Co-Optimization
NN: Neural Network

Introduction

WP2 aims to provide experimental data and extracted parameters from device fabricated in WP1 for the model validation in WP3, through extensive and specific characterizations on a wide range of device geometries operating under a wide range of bias conditions. Electrical reliability tests will be performed to gather hardware data for the reliability-aware design tasks in WP3 and WP4. Additionally, WP2 will estimate ultimate device dimensions achievable through extrapolation at device level, leveraging the design flow developed in WP3 by taking into account the extracted values of device parasitics.

This report focuses on one of the two first characterization and parameter extraction methods of this WP, which is S-parameter measurements and de-embedding methods for extraction of parasitic elements of the test-structures (see Table 1 below).

Table 1: Description of deliverables of WP2 and their topics

Label	Est. delivery date	Description	Partners	Type	DL
D2.1 D2.2	M29 M40	Thermal impedance and trap extraction	UBx, LAAS	R	PU
D2.3 D2.4	**M26** M44	**Parasitic element extraction**	**UBx, LAAS**	**R**	**PU**
D2.5	M56	Report on power-delay/energy-delay products at device-level	UBx, GTS, LAAS	R	PU
D2.6	M56	Report on extrapolated 3D logic cell performance to realistic dimensions	GTS, UBx, INL	R	CO
D2.7	M50	Report on VNWFET reliability tests and failure mechanisms	UBx, LAAS	R	PU

IMS laboratory at the University of Bordeaux has a strong experience in characterization, parameter extraction and modeling of nano-scale electronic devices. For the WP2, which is dedicated to parameter extraction of the gate-all-around (GAA) JL-VNWFET devices, different conventional as well as novel methods of characterization were explored. For this deliverable, particular focus was on the characterization of both passive and transistor test structures, in order to accurately extract parasitic elements external to the transistors that form interconnects with the RF ground-signal-ground (GSG) pads designed for on-wafer measurements.

In the context of emerging technologies for new computing paradigms such as neural networks (NN), vertical nanowire field effect transistors (VNWFET) are a promising technology owing to their naturally 3D architectures [1]. For circuit design using such a 3D emerging technology, it is necessary to build new and accurate compact models to capture the static and dynamic behavior of the device [2]. However, on-wafer test structures of the devices contain many parasitic elements introduced by the RF pads and interconnects that are necessary to probe the devices under test (DUT). The standard procedure to characterize the parasitic effects of a device at high frequencies can be divided into two parts. Firstly, the measurement system needs to be calibrated so that the reference plane is at the probe tips. This can be done using standard calibration techniques such as SOLT (Short-Open-Load-Thru). At this point, all the parasitic elements associated with the pads and interconnects are still included in the measurements. In the second step, S-parameters of the open and short structures are measured which are then used to remove the parasitic elements external to the DUT, through a subtraction process known as de-embedding [3].

Although the process of parasitic extraction is widely used in technologies targeted for high frequency applications, this process can also be applied for technologies such as the VNWFET that are mainly designed for computing applications to improve the modeling accuracy, which normally just relies on DC measurements [1]. Moreover, an accurate modeling of the parasitic elements allows the designer to optimize the 3D layout of the logic circuits and interconnects, thereby improving performance metrics such as compactness and energy-delay product of the technology.

In the scope of T2.2 of the FVLLMONTI project WP2, the following objectives are targeted:

- **To develop a methodology for extracting extrinsic interconnect parasitic network of the RF test-structures**
- **To use predictive E-M simulation for virtually exploring other test-structures for accurate and efficient de-embedding of the intrinsic transistor parasitic elements.**

Extraction of small-signal equivalent circuit for de-embedding of 3D vertical nanowire transistor

I. EXPERIMENTAL DETAILS

RF test-structures:

For the de-embedding of the transistor test fixtures, open structures were designed and fabricated using the same process and on the same wafer as the VNWFETs [4]. The open device consists of all the interconnecting elements leading up to the transistor terminals. Figure 1(a) and (b) show the open structure containing the RF pads, where the absence of the active device can be observed. For the demonstration of the de-embedding process, a VNWFET consisting of 81 nanowires in parallel with a diameter of 17 nm each was selected. A simplified sketch of the interconnected transistor test-structure can be seen in Figure 1(c).

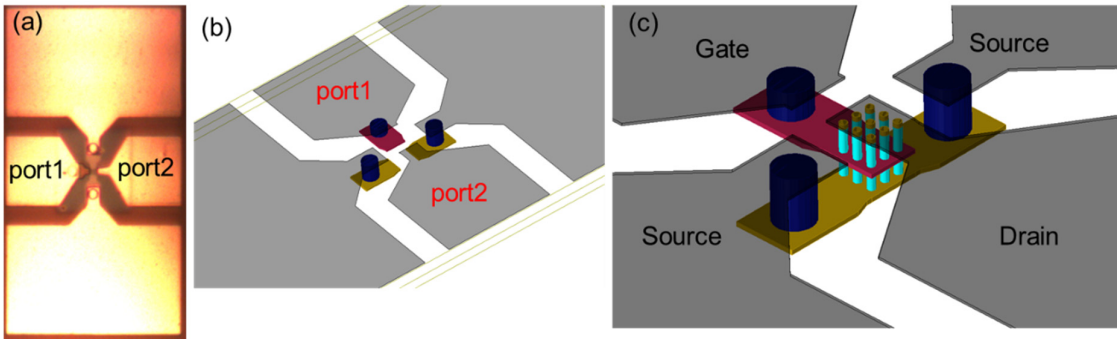

Figure 1: (a) Open structure for S-parameters measurements, (b) a 3-D view of the open structure designed using ADS MOMENTUM and (c) illustration of the VNWFET test-structures with interconnects showing the nanowires.

On-wafer S- parameter measurements:

The on-wafer S-parameters were measured using a Vector Network Analyzer (VNA) from Rohde & Schwarz up to 40 GHz, and a source monitor unit, Agilent 4142B, connected via a bias-tee. A second test bench that allows S-parameter measurements up to 110 GHz, Agilent® E8361 PNA, was used for the open device to ascertain the credibility of the measurements. For both measurement setups, a Short-Open-Load-Thru calibration was performed to set the measurement reference plane at the probe tips. The transistor and the Open test structures were measured using Ground-Signal-Signal RF probes with a 100 µm pitch.

II. METHODOLOGY

Electromagnetic simulation

The 3D view of the open device constructed for EM simulations is shown in Figure 1 (b). The ADS-Momentum EM simulator was used for the computation of the S-parameters of the provided layout. To eliminate manual errors, the layout was imported into ADS using the same GDSII file provided by LAAS-CNRS that was used for the fabrication process. The electrical properties of the material layers were set based on the fabrication process [4]. A cross-section of the materials stack is shown schematically in Figure 2(a), while Figure 2(b) shows the substrate definition used for the EM simulation with each material layer and their properties defined exactly as in the real devices. Figure 3(a) shows the 3D OPEN test-structure and the RF pad layout constructed using Momentum E-M simulator and in Figure 3(b), a comparison between the measured and the EM simulated S-parameters of the open device is shown. The EM simulation results exhibit very good agreement with the measured data up to 40 GHz. Considering that an open structure can be represented by a π-network consisting of three capacitors, the values of these capacitances were extracted from the Y parameters, which were obtained using the standard S to Y parameter transformation method.

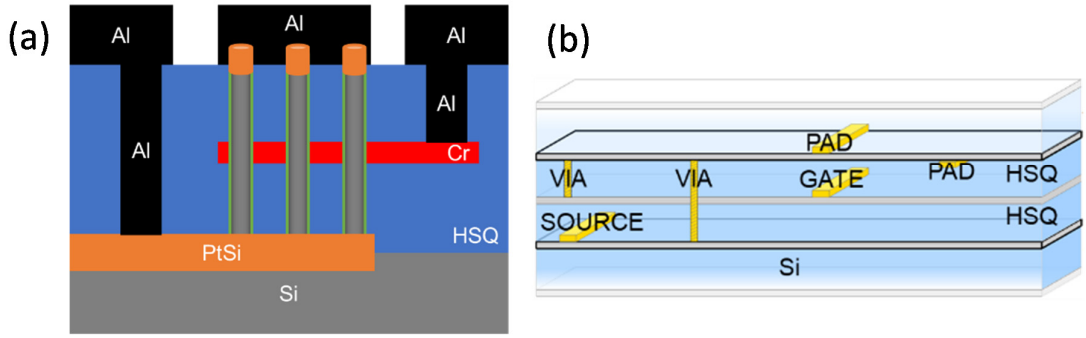

Figure 2: (a) Cross-section of the transistor showing the vertical stack of material layers, and (b) the substrate definition on ADS for EM simulation.

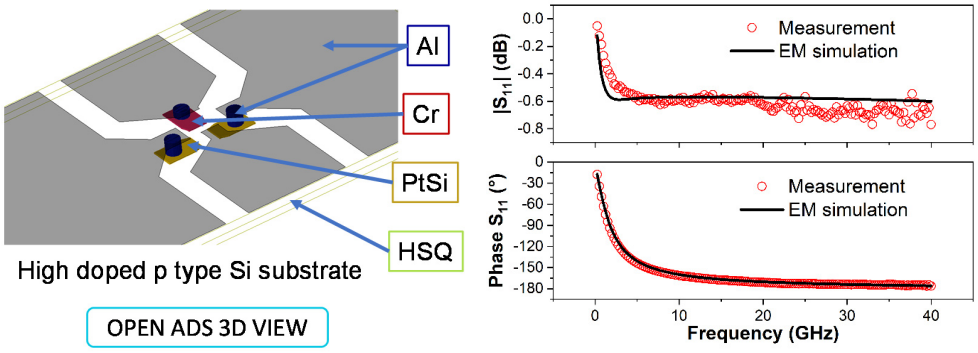

Figure 3: (a) OPEN RF test-structure generated using ADS MOMENTUM; (b) Comparison of S-parameters from measurements and electromagnetic simulation for the open test structure.

The extracted open pad capacitances are shown in Figure 4 for both measurements and EM simulation. The capacitances obtained from the second measurement setup (up to 110 GHz on-wafer measurement), that reaffirmed the first measurement results, are presented as C1_MEAS_110G, C2_MEAS_110G and C12_MEAS_110G respectively. The capacitance C1 extracted from the EM simulation showed good agreement with the measurements beyond 10 GHz. However, below 10 GHz, discrepancies can be observed that might be related to the limitation of EM simulation in reproducing all the details of the fabricated

structures. This indicated that the measurement of the open device below 10 GHz cannot be modeled as a simple π-network. A more complete and lumped model was then investigated taking into account the EM simulation of different sections of the complete open structure and then reconstructing virtual structures for more precise and complete description of the parasitic network.

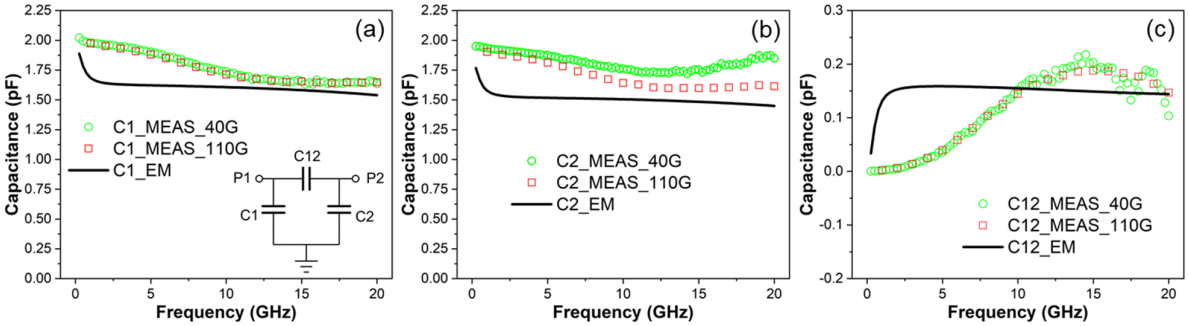

Figure 4: Open structure capacitances extracted from measurements and EM simulation up to 20 GHz. (a) C1, (b) C2 and (c) C12. The inset in (a) shows the equivalent π-network.

Constructing the distributed equivalent circuit of the interconnects

To construct the small-signal equivalent circuit (SSEC) of the open device, EM simulations of different sections of the complete structure were performed to estimate their individual contributions. The pad was considered as an LC network in series with a contact resistance and a π-network was used to model the coupling capacitances between the gate, drain, and the source accesses. The pad capacitance and impedance are estimated from the EM simulations of the virtual OPEN_PAD and SHORT_PAD structures presented in Figure 5(a) and (b), respectively. The coupling capacitances are obtained from the OPEN_DUT shown in Figure 5(c). The extracted elements are then combined to construct the distributed circuit 'model1'.

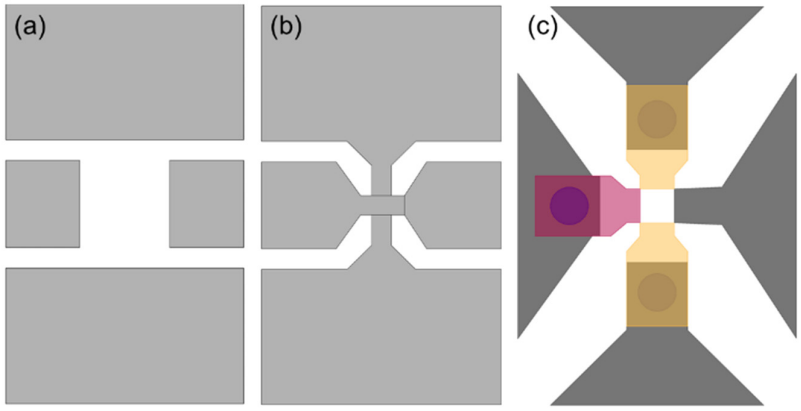

Figure 5: Virtual structures for the EM simulation, a) OPEN_PAD, b) SHORT_PAD and c) OPEN_DUT.

The capacitance C1_MODEL1 in Figure 6, extracted from 'model1', does not match well with the measurement data. This means that not all parasitic effects were accounted for, and a more detailed circuit is required [5]. Analyzing the device layout and the fabrication process, one can identify that substrate parasitic effects might be present due to (i) a low silicon substrate resistivity [4] and (ii) the absence of a ground shield metal underneath the signal pads [6]. The substrate parasitic elements introduce a lossy path, C_{pad2}-R_{sub}-C_{pad3}, shown in Figure 7 along with a fringe capacitance C_{pad1} [7]. The final SSEC is presented in Figure 7, denoted as 'model2'. The values of the components in the distributed circuit were a mix of values estimated mathematically from the physical dimensions and material properties of the device as well as from

EM simulations. Finally, the capacitance C1_MODEL2 extracted from the SSEC 'model2', as already presented in Figure 6, shows an excellent agreement with the measurement.

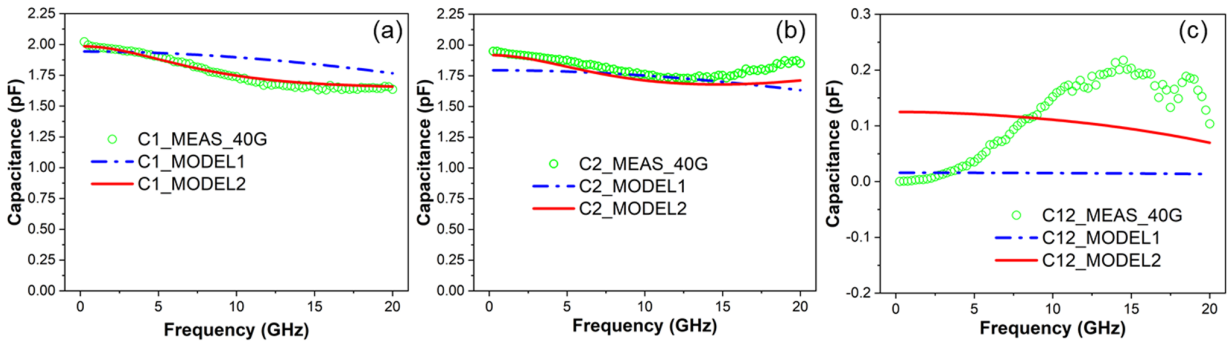

Figure 6: Capacitances as a function of frequency extracted from measurements and electrical simulation up to 20 GHz. (a) C1, (b) C2 and (c) C12.

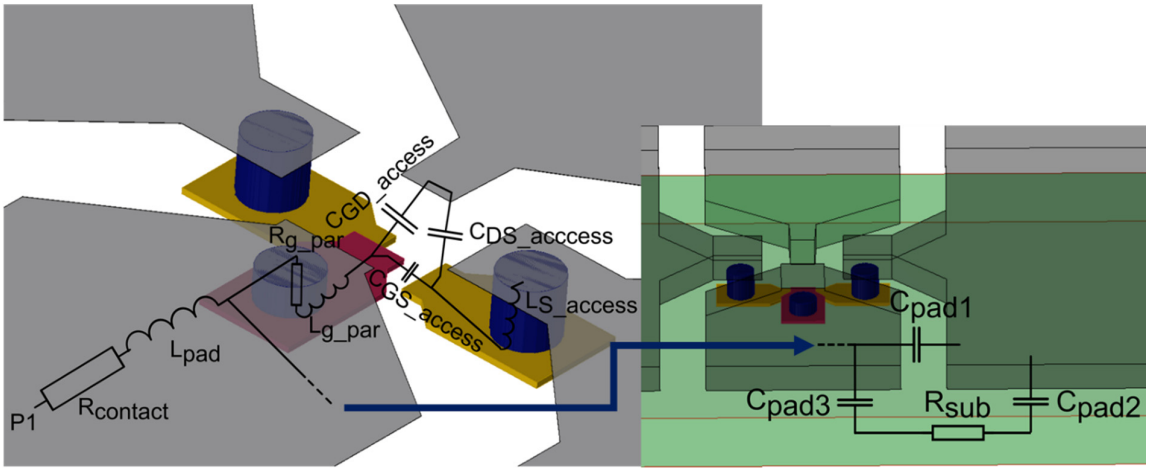

Figure 7: 3D view of the distributed model.

Transistor de-embedding

Two different de-embedding methods were used in this study. The first one is a simple open de-embedding process where the Y-parameters of the open device are subtracted from those of the transistor, referred to as OPEN_deemb. The second approach is based on the methodology described in [8], referred to as the access-modeling based de-embedding (AM_deemb) henceforth. For this, ABCD matrices were used to remove the gate and drain parasitic access contributions, for which the matrix [$A_{transistor\_meas}$] of the complete transistor measurement (including the parasitic effect) was multiplied by the inverse of the matrices [A_{gate}] and [A_{drain}], obtained from the equivalent circuit in Figure 8,

$$[A_{transistor1}] = [A_{gate}]^{-1} \times [A_{transistor\_meas}] \times [A_{drain}]^{-1} \quad (1)$$

The Y-parameters of the C_{GD_access} (Figure 8) were then subtracted from the Y parameters obtained from the ABCD-to-Y transformation of matrix $[A_{transistor1}]$ in (1) as,

$$[Y_{transistor2}] = [Y_{transistor1}] - [Y_{C_{GD\_access}}] \quad (2)$$

Y-to-Z parameter transformation is then performed on $[Y_{transistor2}]$ and subsequently the impedance L_{S_access} (Figure 8) was removed by subtracting its Z-parameters:

$$[Z_{transistor\_deemb}] = [Z_{transistor2}] - [Z_{L_{S\_access}}] \quad (3)$$

The final transistor S parameters were obtained from the transformation of the $[Z_{transistor\_deemb}]$ parameters obtained from eq. (3).

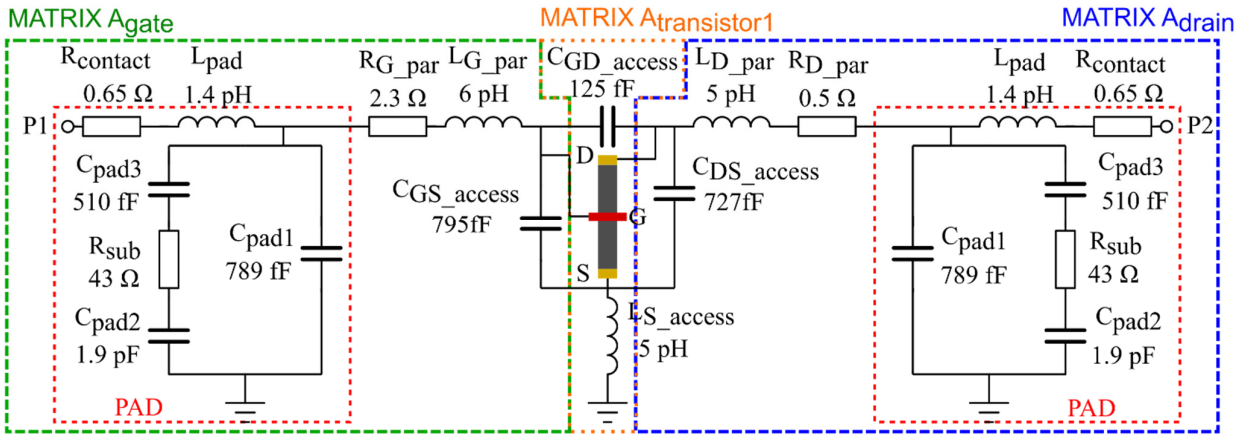

Figure 8: Electrical equivalent circuit representing the parasitic elements obtained from the open test structure that is used for the de-embedding of VNWFET.

III. RESULTS

The gate and drain capacitances, C_{GS} and C_{DS}, obtained from the de-embedded Y-parameters of the transistor at a V_{GS} of -1 V and a V_{DS} of -0.1 V are shown in Figure 9. The data was truncated at 20 GHz since the VNWFET has no RF gain at higher frequencies and the measurement noise becomes dominant. The C_{GS} obtained from the AM_deemb has a mean value of 37 fF compared with 48 fF for the OPEN_deemb. The C_{DS} shows a flat value between 5 and 12 GHz for the AM_deemb, while an unphysical negative value was obtained from the OPEN_deemb. The frequency-dependent increase in C_{DS} above ~ 12 GHz is an indicator of the limitation in the de-embedding method, even though the new proposed method provides more physical results compared with the conventional method. Designing new short and open test-structures with different reference planes would certainly help in better modelling of the entire network of transistor interconnects. Consequently, adequate de-embedding methods and corresponding test-structure designs would be developed for a more accurate extraction of the transistor model parameters.

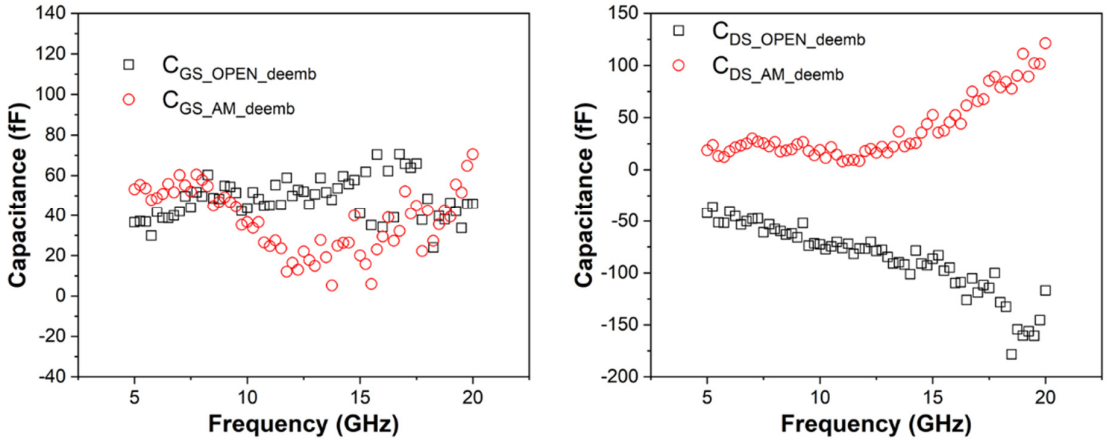

Figure 9: Small signal capacitances as a function of frequency for the de-embedded transistor at a V_{GS} = -1V and V_{DS}= -0.1V.

Conclusion

In this study, the **small-signal equivalent circuit of the VNWFET interconnects** was accurately extracted by using the measurements from the open structure and predictive EM simulation. Adding the substrate parasitic network to the distributed SSEC is crucial for higher accuracy of de-embedding since the capacitance of the open device is more than the intrinsic capacitance of the transistor. The extraction of capacitances could be achieved up to 20 GHz, demonstrating a promising efficiency of our proposed method. In the future scope of this study, the extracted values of the gate capacitances will be verified from 3D TCAD simulation of the transistors and several open and short devices with new layout designs will be fabricated to validate this de-embedding approach.

This report also demonstrates that a comprehensive **experimental framework for the assessment of dynamic behavior of the JL-VNWFETs** is in place within the scope of WP2. The extracted parasitic interconnect network as well as transistor capacitive elements are crucial for estimating the performance of the intrinsic transistor and hence for the compact modeling activities in WP3. Moreover, in view of the Milestones 4 and 12 (Table 2), the **parasitic elements play an important role in estimating the EDP and PDP** accurately, both at transistor and logic circuit level for transient AC simulations and for achieving the DTCO goals. Naturally, the parasitic extraction method and results directly contribute to the EDP evaluation associated with KPI4 (Table 3: Extract of the KPI table from DoA Annex 1 part B 3).

Table 2: Extract of the Schedule of relevant Milestones from DoA Annex 1 part A

Milestone number[18]	Milestone title	Lead beneficiary	Due Date (in months)	Means of verification
MS4	First set of VNWFET electrical parameters First estimation of cell performance	1 - UBx	M32	PDP and EDP using measurements and compact model; Prediction of ultimate device dimensions using DTCO
MS12	Design-technology co-optimization flow validated	2 - UBx	M44	Calculated parasitics fit experimentally extracted resistances and capacitances within a 10% error margin

Table 3: Extract of the KPI table from DoA Annex 1 part B

Key performance indicators (KPIs)	State of Art (SOA)	FVLLMONTI	OBJ
KPI4: EDP assessment for JL VNWFETs, I_{ON} of at least 300 µA/µm at a supply voltage below 0.9Vwith scaled gate length	No demonstration for scaled gate and/or p-type device	Scaled dimension and supply voltage with efficient drive current	**OBJ2** MS2 MS4

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