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DOCUMENT ABSTRACT

In this deliverable, we described the development of elementary ambipolar nanowire device demonstrators in FVLLMONTI. Most importantly, we report process flows and characterization data for two novel concepts experimentally demonstrated within FVLLMONTI: a.) the common-body reconfigurable field effect transistor for flexible current routing, as executed on a two-dimensional cross-shape channel geometry and b.) the ambipolar U-Shape transistor with vertical $NiSi_X$ contacts.

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LIST OF ACRONYMS / GLOSSARY

D: Deliverable
M: Month of the project
P: Partner
WP: Work Package
PU: Public
V: Version
FET: Field Effect Transistor
PC: polarity-controllable
RFET: Reconfigurable Field Effect Transistor
CMOS: Complementary Metal-Oxide-Semiconductor
PG: program gate
CG: control gate
MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor
SOI: Silicon-on-Insulator
GAA: Gate-All-Around
JL: Junction-Less
RF: Radio Frequency
TCAD: Technology Computer-Aided Design
DTCO: Design-Technology Co-Optimization
BOX: Buried oxide
GSG: Ground-signal-ground
VNA: virtual network analyzer
SOLT: Short-Open-Load-Thru
ISS: Impedance Standard Substrate
SEM: scanning electron microscope
EBL: electron beam lithography
ICP: inductively coupled plasma
RTA: rapid thermal annealing
NW: nanowire
VNW: vertical nanowire
ALD: Atomic layer deposition
TEM: transmission electron microscopy
CS-RFET: Cross-shape Reconfigurable Field Effect Transistor

1. Introduction

The polarity of a classical Field Effect Transistor (FET) is fixed to either n-type or p-type by the underlying materials and fabrication process. In contrast, ambipolar polarity-controllable (PC) transistors can be used in one of the two modes through only electrical signals, either statically or dynamically reprogrammed at run-time. Due to this transistor-level reconfigurability, PC devices are typically named Reconfigurable Field-Effect Transistors (RFETs) in literature. The novel technology has the potential to overcome some of the fundamental limitations of conventional Complementary Metal-Oxide-Semiconductor (CMOS) technologies, given such a higher level of logic expressiveness, reduced costs per basic implemented logic function are foreseen.

I. RECONFIGURABLE FET OPERATION

The Reconfigurable Field-Effect Transistor (RFET) operates as an electronic device capable of seamlessly switching between n-type and p-type operation modes employing electrostatic doping that modulates source/drain Schottky barriers acting as carrier injection sites. This concept involves the generation of mobile carriers through an external potential, allowing for a reversible alteration of majority charge carriers (electrons or holes) in the intrinsic channel. Devices employing this principle are known under various names, like polarity-controlled FETs, dually active channels, etc. Regardless of nomenclature, these devices share a common feature: at least two independently controlled gates that electrostatically dope the channel. One, the so-called polarity gate (or program gate, PG) controls the injected carrier type (i.e. the conduction mode), while the control gate (CG) simply switches the transistor on and off (Fig. 1.). This ultimately means that n-type/p-type polarity control is achieved by splitting the single gate of a transistor based on the doping-free ambipolar base technology into two gates able to render the two separately accessible unipolar characteristics. Unlike conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), where ungated channel segments lead to a loss of the inversion channel and, therefore, of channel conductivity, the separation of the single gate of a MOSFETs into the two or more top gates of an RFET actually allows for independently tuning electron and hole currents without degrading the channel characteristics, given a reasonable gate pitch, because of the different doping criterium.

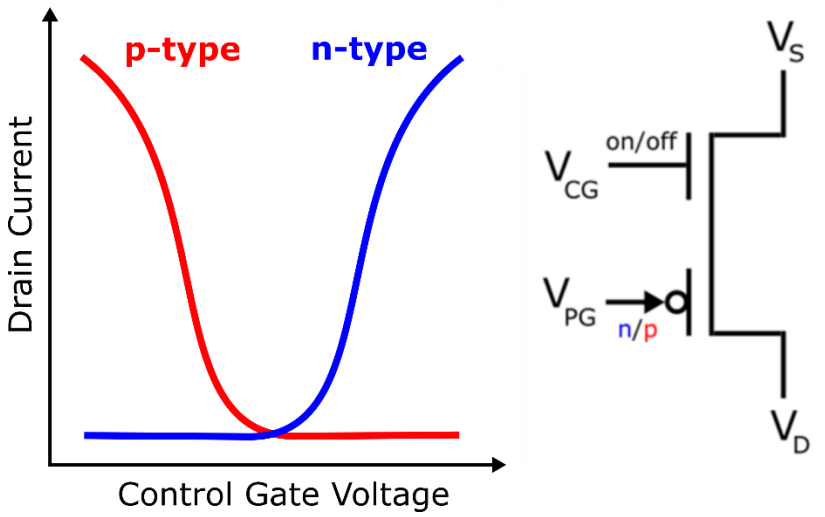

Figure 1. Conceptual operation of a reconfigurable field-effect transistor (RFET). At least two independent gate electrodes are employed to steer the conduction in am ambipolar channel. The PG sets the polarity to either p- or n-type, while the CG switches the transistor on or off.

II. PROJECT RELEVANT RECONFIGURABLE FIELD EFFECT TRANSISTORS VARIANTS

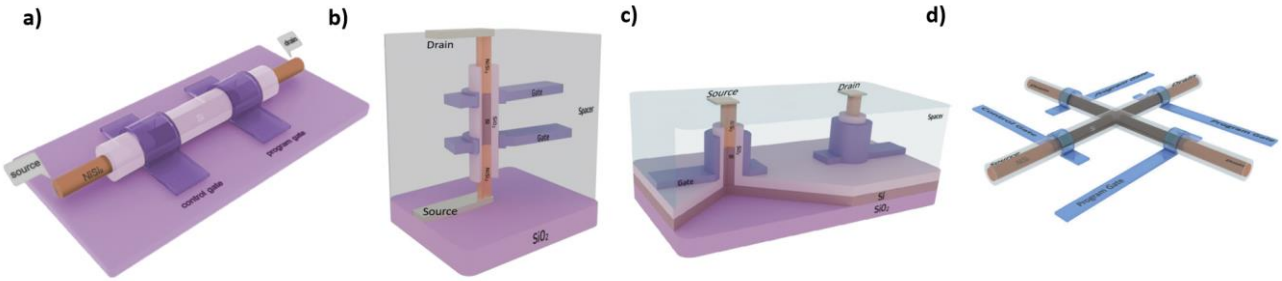

Figure 2. 3D schematics of a RFET in different architectures. a) Double- gated simple planar, b) true-vertical, c) U-shape and d) cross-shape RFET.

The characteristics and properties of planar dual-gated RFETs (Fig. 1a) are nowadays well established [1]. The device concept has been demonstrated to show potential for analog circuit applications [2], hardware security[3], and neuromorphic systems[4] and. Thus, it can serve as a powerful CMOS add-on functionality. It has been demonstrated that a multitude of circuit functionalities can be mapped onto the same physical logic cell, simply by applying the right signal configuration [6]. This might be a key feature to enable a vertical stacking of logic functions once a true vertical RFET devices (Fig 2b) has been realized. In addition, the avoidance of impurity doping for the channels, as well as the changed transport behavior help to facilitate arbitrary structures in a 3D environment. This way, extended signal routing capabilities particularly relevant in the field of neuromorphic computing can be added, which were experimentally demonstrated for the first time within FVLLMONTI through the development of the Cross-Shape RFET (Fig. 2d). Transferring these capabilities to a 3D technology holds the promise of greater circuit complexity with a smaller device footprint [7]. For this reason, a U-Shaped RFET was conceptualized and its concept is reported in Fig. 2c, where the shared Silicon-on-Insulator (SOI) body can be used as common-channel similar to the one demonstrated in the cross-shape RFET. This intermediate step towards the fully 3D integrated structure Gate-All-Around (GAA) transistor with enhanced gate coupling, reduced RC effects, and superior sub-threshold swing performances, is the main technological aim of this deliverable as it allows to simplify the process challenges with respect to complex top/bottom contacts generation and stacked-gate alignment processes (which are under development for Junction-Less (JL) transistors explored in FVLLMONTI) while still being able to characterize a reconfigurable gate-all-around vertical nanowire transistor. Thus, the remainder of this deliverable covers the following achievements:

- Planar RFET Test-structures for Radio Frequency (RF) characterization and modeling support
- Cross-Shape RFETs, demonstrating a new device concept facilitating extended operation capabilities, ready for carryover in true 3D geometries
- A Technology Computer-Aided Design (TCAD)-aided scaling study transforming the cross-shape concept to a U-shape transistor with a common SOI body
- An elementary process flow for said vertical U-shape ambipolar transistors

2. Planar RF-Test Structures

RF measurements can be used to access the intrinsic parameters of emerging devices in order to server as input data for the development of compact models. As establishing a vertical process flow takes considerable time, early analysis in FVLLMONTI was executed on the well-established planar technologies to yield input parameters for modeling work packages. Planar devices offer an easy way to scale the device dimensions, allowing all contacts and measurement pads to be in plane with the channel area. The data gathered from

planar structures can be adapted/extrapolated to GAA geometries employing the Design-Technology Co-Optimization (DTCO) framework established in FVLLMONTI.

I. PRELIMINARY: SUBSTRATE RELATED CHALLENGES

Notably, all reconfigurable devices explored in FVLLMONTI are built from SOI wafers. The buried oxide (BOX) layer on a SOI wafer provides very good DC isolation and allows the fabrication of PC/RFET devices. In a planar design, the devices and measurement pad can be fabricated in a single metal layer process. However, for RF measurements, this presents a challenge in terms of coupling the signal through the substrate. We then investigated the effect of substrate resistivity on open pad test structures that can be used to de-embed the devices. Three different wafers were studied, and the main characteristics are shown in Figure 3.

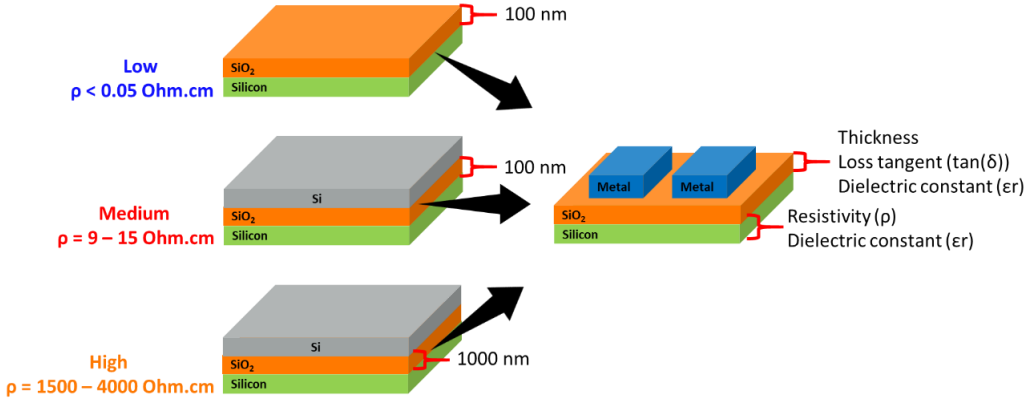

Figure 3. Different substrate wafers used for the fabrication of the structures (left) and a schematic of an open structure with the main properties of each layer (right). The silicon layer was etched away before the metal deposition for the medium and high resistivity wafer.

II. SIMPLE PLANAR RF-TEST STRUCTURES FOR RFETS

Unlike DC measurements, where single probes touching a metal pad are sufficient to make electrical contact and measure devices, a typical RF setup involves the use of special probes, usually with a coaxial cable at one end and a ground-signal-ground (GSG) probe tip at the other. It is necessary to design and fabricate on wafer pads that match the characteristics of the selected probe. A common source measurement configuration is used for a typical FET, i.e., the gate and drain are connected to the signal terminals, while the source is grounded. Before measuring the transistor, it is necessary to have de-embedding structures that allow us to remove the parasitic effect of pads and metal interconnections, placing the reference plan of the measurement at the transistor level. As already mentioned, everything is done in a single metal layer. For the present work, an open pad structure carries most of the parasitic effects and has been used to study the effects of substrate resistivity. Figure 4 shows the layout of the open pads with the GSG structure. The pad dimensions used were compatible with 100 µm pitch probes.

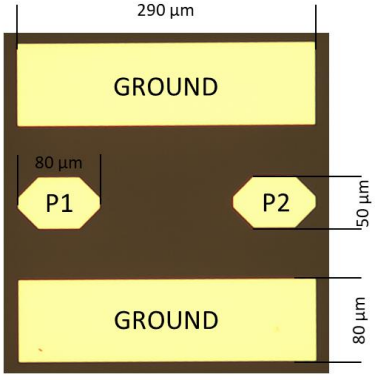

Figure 4. Optical image of the fabricated open pad structure with the dimensions of the pads.

III. CHARACTERIZATION OF RF-TEST STRUCTURES

The characterization was performed by measuring the S-parameters with a virtual network analyzer (VNA) ranging from 250 MHz to 24 GHz, using |Z| Probe® RF probes with 100 µm pitch. The measurements were preceded by a Short-Open-Load-Thru (SOLT) calibration done on an Impedance Standard Substrate (ISS). The results of the open pad structures fabricated on the three different substrate resistivity are presented in Figure 5. The high resistivity wafer presents a lower capacitance effect, as shown by the S_{11}, and reduced cross-talk, S_{21}, at lower frequencies, making it the most suitable choice for transistor fabrication [8].

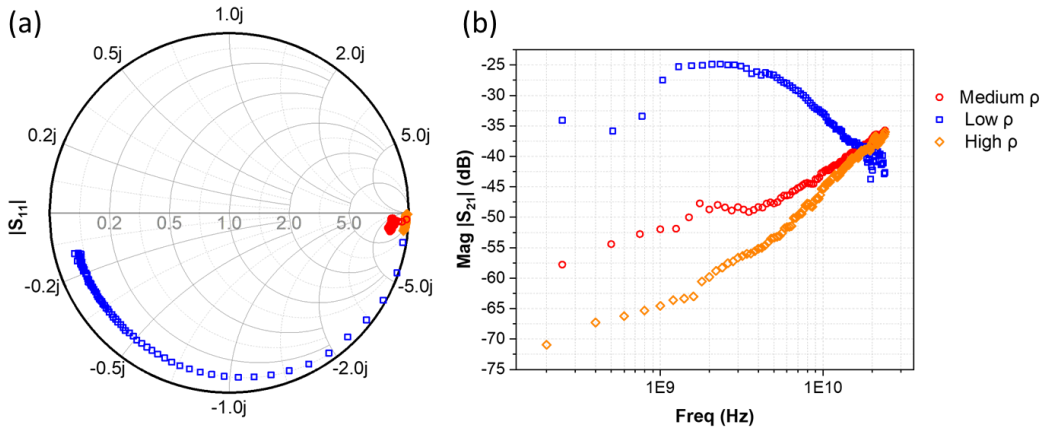

Figure 5. S-parameters for the open pad structures from measurements for different resistivities ρ. (a) reflection coefficients S_{11} and (b) transmission parameter, S_{21}, in magnitude.

IV. HORIZONTAL RFETS WITH NANOCHANNEL VARIATION

As the development of the vertical U-shape RFET requires a significant amount of time, horizontal devices were fabricated to serve as input point data for constructing a compact model for the technology. Figure 6 shows the layout of a horizontal RFET with the necessary pads for RF measurements. Compared to the open pad design, a modification was made to the ground pads to allow the placement of the second gate pad, which is used to select the transistor's working mode. To gain insights into the scalability of these devices and increase the on-current, devices with varying numbers of nanochannels (1,5,15 and 25) were fabricated. Figure 7(a) shows an scanning electron microscope (SEM) image of a 25-nanochannel structure before the fabrication of the gate, while Figure 7(b) displays the transfer curve (gate voltage vs. drain current) for all devices. The non-linear increase in drain current with the number of channels can be attributed to the non-homogeneous length of the silicidation. Characterizing these devices at RF aims to extract intrinsic parameters, such as the gate capacitance, which is an essential input for the compact model. Those results are reported in another deliverable.

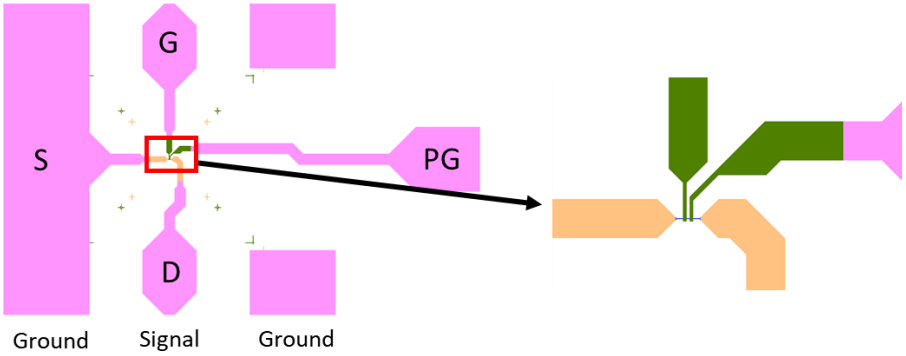

Figure 6. Layout of a horizontal RFET and the pads for RF measurement. Highlight presenting the position of the dual gate on a single nanochannel device.

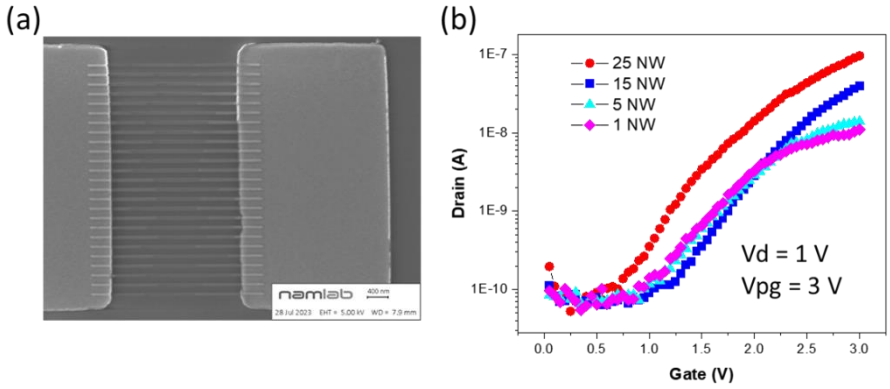

Figure 7. SEM image of a 25 nanochannel structure before the fabrication of the gates (a), and the transfer characteristics for the RFETs with different numbers of nanochannels (b).

3. Common-Body RFET on a Cross-Shape Channel

I. CONCEPT OF COMMON-BODY TRANSISTORS

The connection of multiple silicon channels sharing a single common body enabled by the SOI technology elegantly allows the production of arrays of independently controlled nanowires. These can serve as parallel source and drain contacts, allowing the entire device to carry a higher current with respect to a single source/single drain device configuration. This way, the current flow in the channel can be adjusted depending on the arrangement of the wires and the selected gate voltages at run-time. To demonstrate the disruptive concept of a common-channel reconfigurable field-effect transistor, a cross-shaped structure is selected as the initial 2D configuration due to its symmetrical nature and ease of fabrication compared to a 3D implementation of the same concept [7]. The fabricated cross-shape reconfigurable field effect transistor is composed of a doping-free common channel with four independent silicided source and drain junctions, a silicon dioxide dielectric layer, and four independent gates aligned on top of the silicide junctions. The pivotal feature that enables the unique device behavior is that RFETs are diffusion-dominated devices, operational even with ungated areas in the middle of the channel. This means that an arbitrary number of source or drain terminals can be connected onto a common body as long as a good gate control is achieved by the fringing fields of the individual gates. This device concept was demonstrated experimentally using planar technology, but it can be extended to a true 3D version, increasing flexibility and strongly reducing area footprint. Through this unique common-channel structure, device-level current routing was exhibited. This device concept has high potential for future signal routing applications and bio-inspired neuronal networks. Further branching the channel into parallel channels and placing additional gates.

II. PROCESS FLOW

The first cross-shape RFETs were realized on a SOI wafer with a 20 nm Si thickness on 100 nm BOX. Four 80 nm wide and 2 μm long nanowire branches with contact pads were patterned in a cross-shape geometry. Electron beam lithography (EBL) technology enables the achievement of precise fabrication as well as good crystalline continuity at the interconnection point [9]. Contact pads were designed to yield higher mechanical strength during the fabrication process of the transistors. Undesired areas were etched with an inductively coupled plasma (ICP) etching process. SiO_2 was selected as gate dielectric layer and grown by a rapid thermal oxidation process. Sacrificial oxide etch was performed by using wet etch for a thinning down the nanowire size and a higher sidewall uniformity. Subsequently, 5 nm oxide growth and N_2 annealing were carried out again in rapid thermal annealing (RTA) oven. The measured channel width of each branch of the cross-shape

nanowires (NWs) is 70 nm after the thinning and oxide growth process. Nickel-silicide junctions were created by a sequential lithography process for contact pad definition, oxide etch, immediate Ni sputtering, and a rapid thermal annealing process. As the silicide length is a temperature and time-dependent process, the resulting silicide length is the same for each interconnected NW as long as the alignment of the nickel pads is precise. Gate contacts were also defined by using lithography and subsequent nickel/platinum gate metal sputtering. Finally, measurement pads were created using a laser lithography step and sputter metal deposition. A simplified process flow with SEM images of key steps is displayed in Fig. 8.

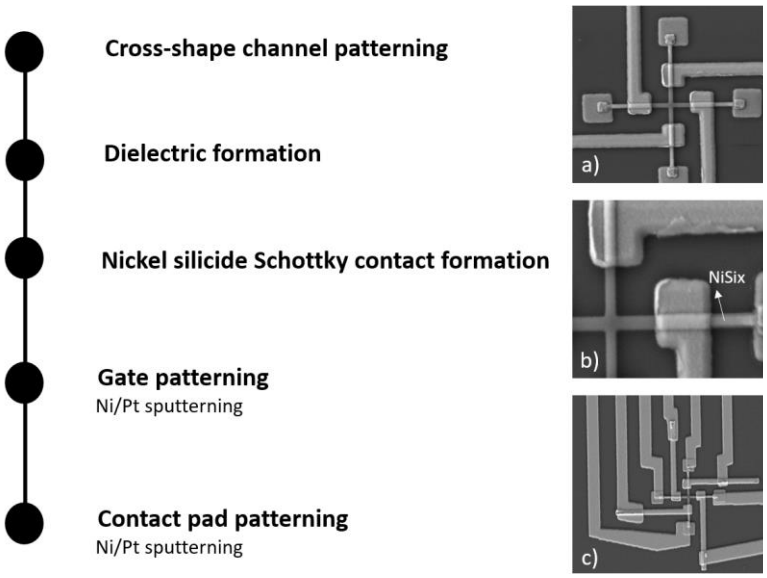

Figure 8. Key process steps route for the fabrication of the Cross-Shaped-RFET. SEM images highlight the most important process steps (a) gate patterning, (b) thermal NiSi formation at all four source/drain contacts and (c) contact patterning.

III. ELECTRICAL CHARACTERIZATION

The cross-shape RFET was built on a continuous intrinsic silicon channel, consisting of four silicon nanowires in a cross-shape layout with four separately gated Schottky junctions as source/drain contacts at each channel end. In the measurement setup, one branch was always kept as drain (D), and the other three branches were selected as individual source contacts (A, B, and C, inset Figure 9). In principle, each branch can be flexibly chosen to fulfill any role. Thereto, a PG is located on top of the drain-sided junction and each source is controlled by an independent CG. The un-gated cross-shaped area in the center serves as the common channel for all current paths. In principle, each individual current path can be assumed to act as double gated (DG)-RFET, which can be programmed to n-type or p-type by blocking the undesired charge carriers. Under the condition of $V_{PG} \geq V_D \geq 0$ V, the positive charge carriers are blocked at the drain side. By applying sufficient voltage to the control gate, electrons at the source are injected into the channel and the device behaves as n-type. The p-channel mode can be obtained by applying negative voltage values. The measured transfer characteristics of each single source branch towards the drain are given in Fig. 9 (a). The measurement was conducted between branches A-D, B-D, and C-D, respectively. In all configurations, D was kept as drain and unconnected branches, and the corresponding control gates were grounded unless noted otherwise. An on/off-ratio larger than 10^5 was achieved at a V_{DS} of |1|V. All Hysteresis-free transfer characteristics were obtained by sweeping the control gate voltage with a constant drain and program gate voltage of 1 V and 3 V, respectively, while the source was grounded. The static routing of the current between the interconnected wires was achieved with a high similarity in the on- and off-current values and relatively symmetric p-and n-behavior originating from the difference in the natural Schottky barrier height for the holes and electrons. An enhancement of the on-current at the drain contact can be observed when multiple sources are operated at the same time as shown in Fig. 9 (b). Connecting one additional source drives more current towards the output as compared to only one source, which is due to the increased number of charge

carriers injected into the channel. It can be observed that a nearly perfect linear increment in on-current is achieved for both n-type and p-type program. P- and n-type output characteristics of a single source and drain configuration (A-D) are presented in Fig. 9 (c) and (d). The measurements were conducted by sweeping the drain voltage with a constant $|V_{PG}|$ value of 3 V and a step increment in V_{CG}. Schottky typical supra-linear increase in current for lower V_D values can be seen for both p-and n-configuration. This behaviour originates from the effect of the drain-voltage on the injecting barrier.

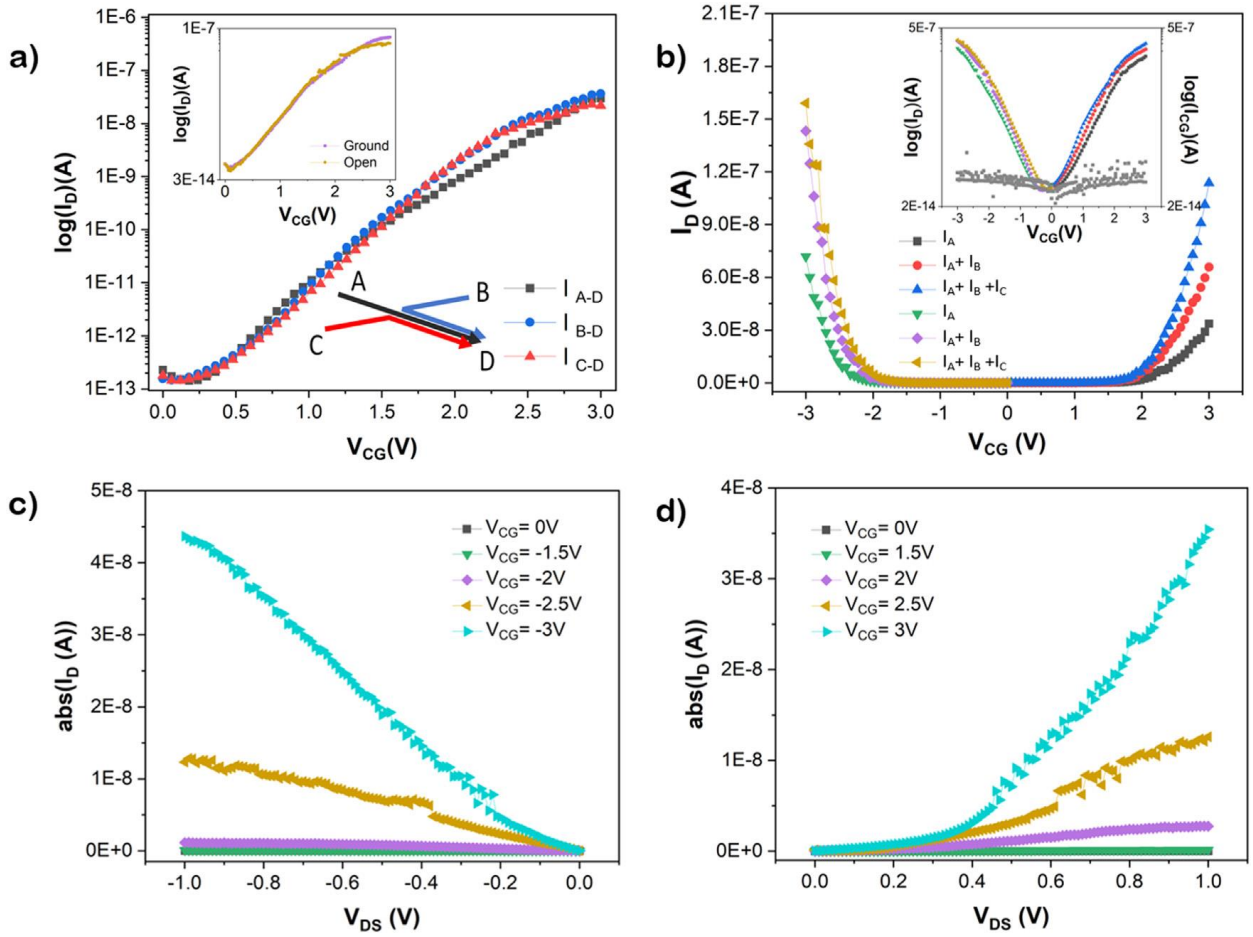

Figure 9. Electrical characteristics of the CS-RFET. a) n-type transfer curve for each branch of the cross-shaped channel, as labelled in the figure. b) n-type and p-type currents for an additive number of channels, showing a linear increase of the drive current with the number of activated channels. c,d) p-type and n-type output characteristics, respectively.

4. TCAD-aided Scaling Study – From Cross-Shape towards U-Shape

TCAD simulations were conducted using the GTS framework to assess the impact of scaling on the cross-shape RFET investigated along the project. Besides, U-shape transistors featuring a denser implementation of the cross-shape RFET structure have also been investigated through TCAD simulation to provide a first evaluation of their hybrid 2D/3D geometry.

I. TCAD SIMULATION OF THE X-SHAPE TRANSISTOR

Figure 10(a) and (b) illustrate the reference cross-shape structure considered in this study and the corresponding simulated structure (2D top view). The structure consists of 4 NWs with dimensions of 70nm width and 10nm height, standing on a 100nm-thick Buried Oxide (BOX) layer. The NWs were isolated from the Program Gates (PGs) by a 5nm-thick silicon dioxide layer, with both layers entirely surrounding the NWs.

An edge-to-edge distance of 500 nm was taken between the 300 nm-long PGs in agreement with the SEM top view. Additionally, NiSi silicide contacts positioned in the middle transverse plane along the PG length were considered to achieve S/D Schottky contacts. Carrier transport within the Si channels was governed by drift-diffusion, while Tsu-Esaki tunneling was considered for carrier injection from the silicide into the Si nanowires. Figure 10(c) shows simulated transfer curves for both types of polarity ($|V_{PG}|$=3V), while Figure 10(d) reports the n-type transfer curves achieved with increasing channel currents. A fair agreement with experimental data is achieved, although results in Figure 10(c) suggest that further refinement of the mobility model parameters for both types of carriers may be required to further improve the agreement with experimental data throughout the Control Gate voltage range.

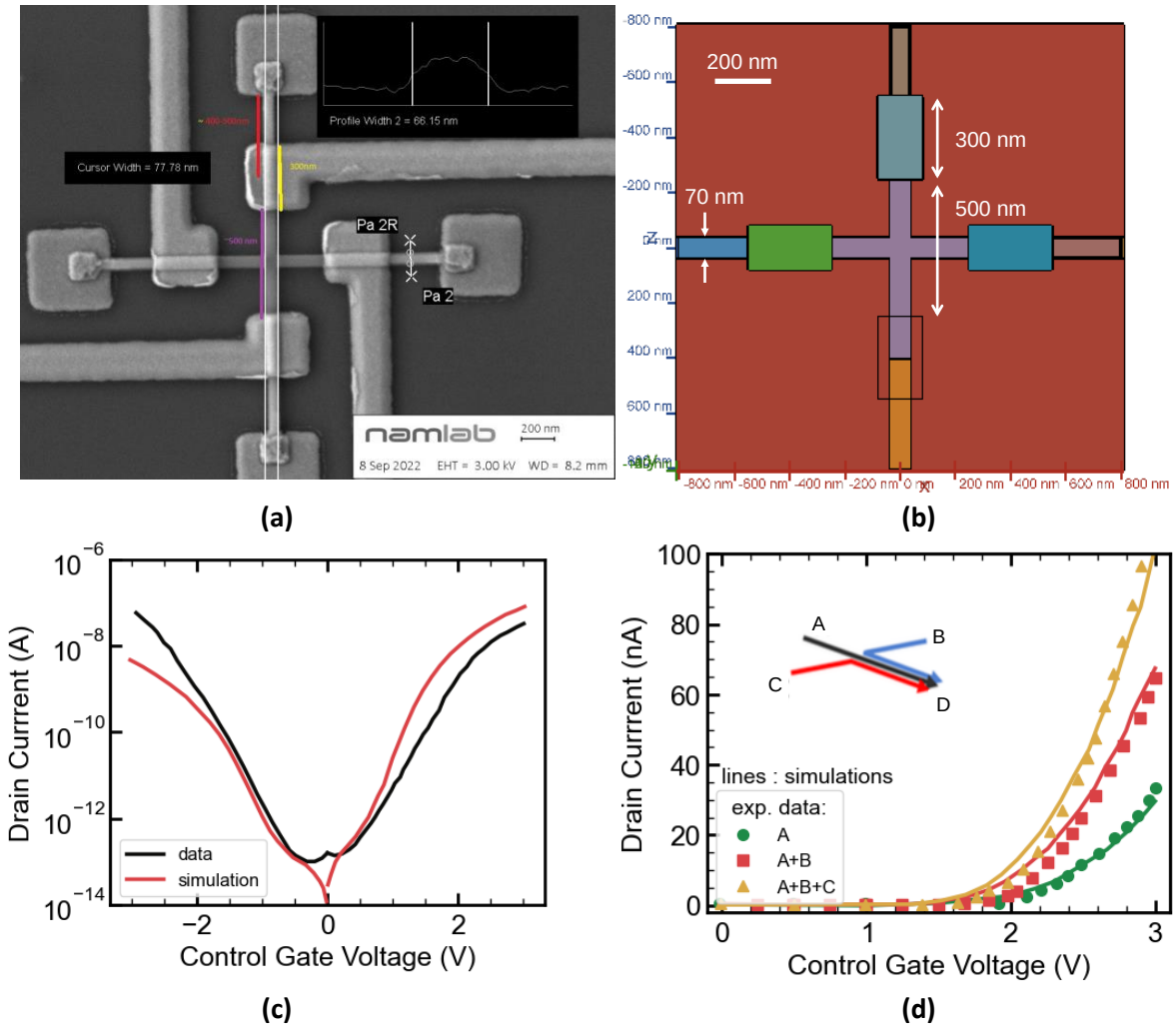

Figure 10. (a) SEM top view of the cross-shape RFET and (b) top view of the 3D simulated TCAD structure using the GTS framework. Comparison of experimental and simulated transfer curves of the RFET at a constant $|V_{PG}|$ value of 3 V and drain voltage $|V_{DS}|$ of 1V (c) for n-type and p-type currents and (d) with increasing channel currents.

II. IMPACT OF SCALING: FROM THE X-SHAPE TO THE U-SHAPE TRANSISTOR

In order to evaluate the impact of scaling on the cross-shape transistor, the gate spacing distance was varied from 700 to 200 nm. A minimum distance of 200 nm was kept in order to prevent contact between neighboring PGs. Keeping the PG length to 300 nm, it must be noted that the minimum distance between the external edges of PGs is 800nm. Figure 11(a) shows the impact of gate-spacing distance on the transfer curve (i.e. n-type configuration). It is observed that gate spacing has a marginal impact on the drain current, the latter being controlled by the conduction band barrier height lying in the middle of the channel, which is not subjected to the electrostatic control of the PGs (see inset). As described more in detail in the next section

of this report, U-shape transistors combining GAA nanowires formed onto a SOI substrate were then considered for TCAD simulations as an evolutionary implantation of the RFET. Figure 11(b) shows a 2D cross-section together with a 3D TCAD view of the simulated structure. The smallest U-shape transistor consists of 2 GAA vertical nanowires (VNWs) raised on an SOI substrate. The VNWs are surrounded by a 5nm-tick SiO_2 layer serving as PG oxide and are contacted at their summit by a nickel silicide to achieve S/D Schottky-contacts. Finally, programming gates (i.e. Source/Drain PtSi Gates) surrounding the base of the NW are used to select the polarity control of the U-shape transistor. It should be added that PG is isolated from the SOI layer by a thin 5nm-thick SiO_2 insulation layer. The U-shape structure features a 10 nm diameter VNW distant from 300 nm (axis-to-axis distance), thus already achieving a denser hybrid 2D/3D implementation of the previous planar cross-shape structure. In order to allow a fair comparison with the simulated cross-shape transistor, simulation parameters were kept identical for the U-shape and the cross-shape structure.

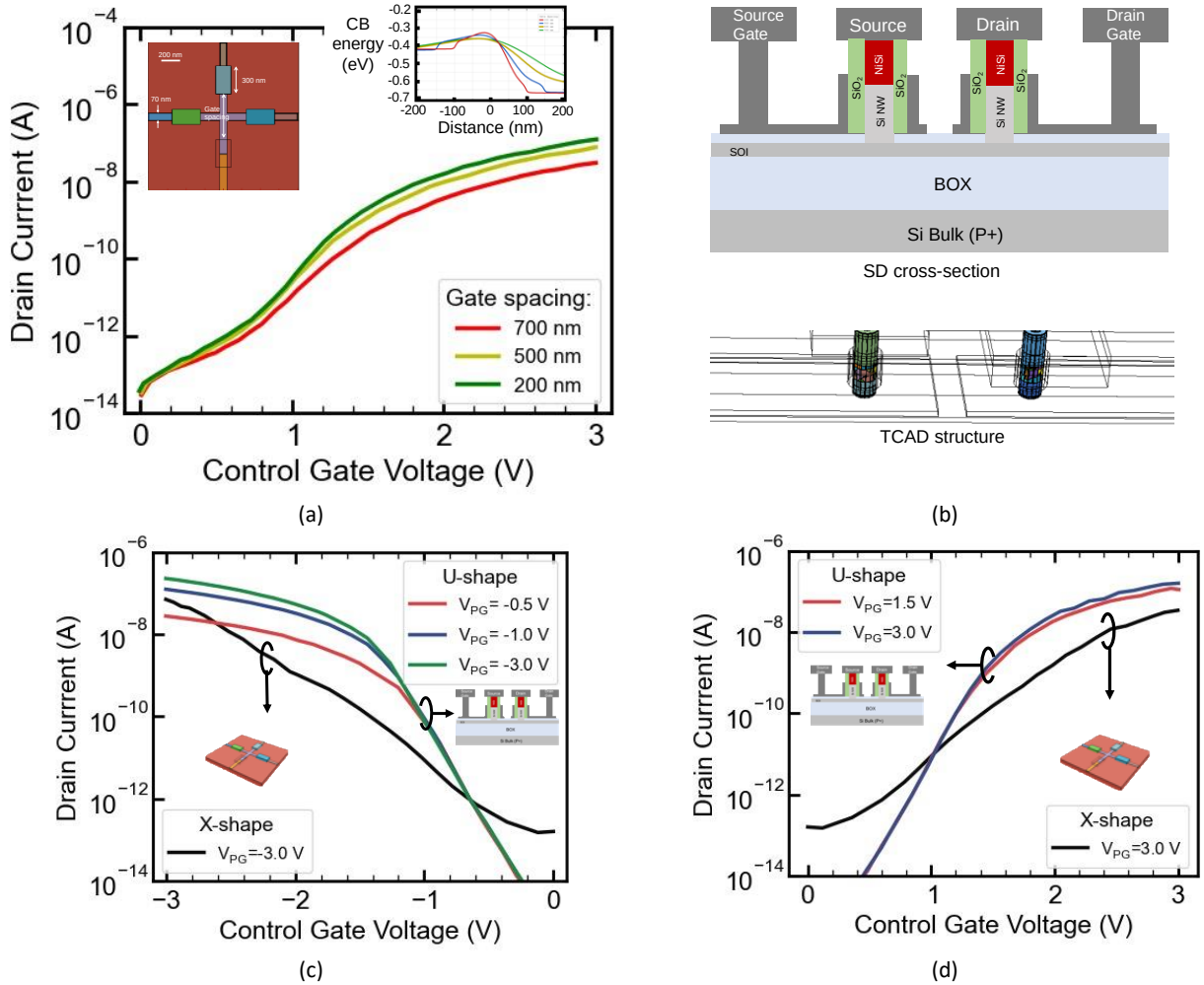

Figure 11. Effects of scaling the RFET and transition to U-shape structures. (a) impact of Programming Gate spacing on cross-shape transfer curves. The inset shows the conduction band height along the NW channel. (b) 2D cross-section of the simulated U-shape structure and 3D view of the TCAD structure. The distance between neighboring nanowires is 300nm. (c) and (d) compares the experimental transfer curves of the cross-shape RFET and the simulated one obtained on the U-shape transistor.

Figure 11(c) and (d) compare transfer curves obtained from the U-shape transistor with electrical data issued from the cross-shape structure for both types of polarity. It must be noted that the U-shape transistor achieves a larger driving current at lower PG voltages and a steeper slope than its cross-shape counterpart. While the larger drain current can be attributed to the reduced distance between the NW as compared to the cross-shape structure (300 nm vs 500 nm) the neat improvement in the sub-threshold current can be attributed to the combined effect of the series SOI channel together with the electrostatic control achieved by the PG through the fringing field through the SOI/PG SiO_2 insulation layer. Combined with the possibility

of further embedding multiple VNW underneath S/D contacts, these simulation results thus provide encouraging indications on the potential of U-shape transistors for future RFET applications.

5. Vertical U-Shape Ambipolar Transistors

To continue miniaturization, transforming the architecture of the transistor from traditional 2D to 3D is one of the most important attempts in FVLLMONTI. Vertical nanowire FETs represent a compelling choice for GAA structures, offering a strong alternative to current FinFET technology. Their vertical design inherently allows for a more compact layout, enabling increased integration density while also providing gate length flexibility. However, manufacturing, particularly contact formation, spacer processing, and process monitoring, remains considerably more challenging than a planar device.

(Polarity controllable) reconfigurable field effect transistors present an opportunity to enhance functionality through selectable n and p-FET polarities. RFETs allow for programmable logic computing of diverse logical functions within the same circuit, achieved by modifying a program signal at the transistor level. Consequently, despite classical scaling, applicable to the RFET concept, there is an augmentation in circuit functionality and flexibility, all while maintaining an equivalent transistor count. Nevertheless, the RFETs facilitating multiple independent gates typically require a larger contact area than classical MOSFETs. The U-shape integration of RFETs effectively addresses challenges related to both the area and contact formation. The U-shape design simplifies contact formation and eliminates the need for individual complex top/bottom contact generation and gate alignment processes, as all gates are placed in the same layer. The device allows for dynamic control over the channel geometry, thereby enabling versatile functionality well-suited for signal processing and reconfigurable computing applications. While U-shape transistors have been studied in simulations [10], [11], [12], here we report the first experimental demonstration. This integration leads to improved performance, primarily attributed to the utilization of vertical nanowires in conjunction with GAA contact geometry. The vertical GAA structure, in particular, enhances the coupling between the gate and the channel, resulting in reduced parasitic RC effects and superior subthreshold swing values. Consequently, this approach also contributes to advancing layout efficiency in semiconductor device design.

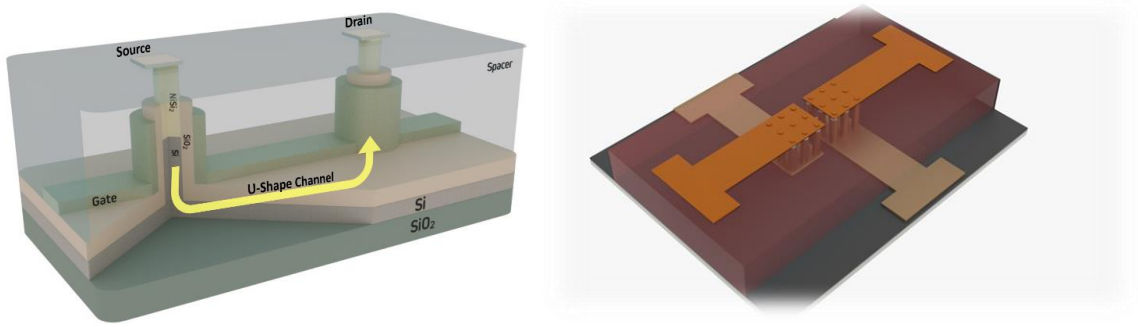

Figure 12. 3D schematic depiction of the a) envisioned U-shape ambipolar nanowire transistor and b) its final polarity controllable realization with independent gates and multiple nanowires per contact.

I. PROCESS INTEGRATION FLOW

The process integration flow for the fabrication of a U-shape ambipolar transistor is outlined in detail in Figure 13. To enhance the on-state currents and for ensuring superior yield, instead of using only two vertical nanowires forming the U-shape, nanowire arrays with a total of 81 nanowires are used for both the source and drain pillars. As already described before, these are connected by their shared bottom channel. For a simplified visualisation, the conceptual version featuring only two vertical nanowires is always considered. The devices are processed on a silicon-on-insulator substrate featuring 160 nm of silicon over 150 nm of BOX. The etching conditions are precisely adjusted to achieve vertical sidewalls, and nanowire heights up to 120

nm. To decrease the roughness of the sidewalls and shrink down the channel dimensions, a rapid thermal oxidation process was performed, and the formed oxide was consequently removed via wet etch.

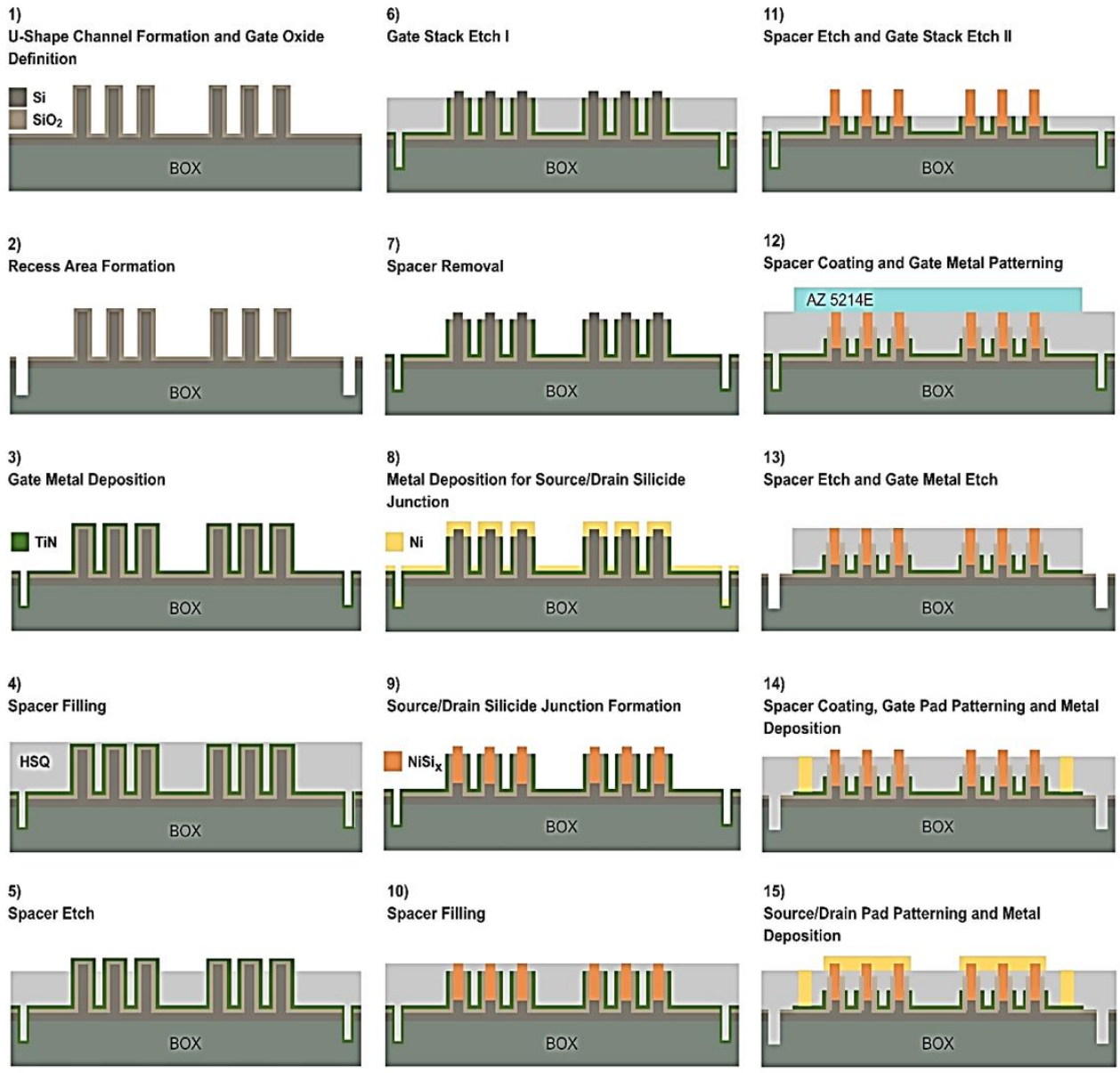

Figure 13. Illustrative 2D cross-sectional schematics depict the key stages in the process integration of a fabricated U-shaped ambipolar SBFET. a) U-shape channel fabrication includes the 50 nm wide EBL patterning of 90 nm thick HSQ pillars, depth limited (120 nm) selective ICP etch of Si-NWs, and thermal oxidation process for thinning-down and a gate oxide formation. b) The photoresist was patterned by using laser lithography to separate the transistors from each other. The photoresist served as a hard mask for the SF6-based ICP etch. c) Atomic layer deposition (ALD) of 12 nm TiN gate metal. d) Spin coating of 180 nm HSQ spacer. e) Precise diluted HF etch of spacer to open the tips of Si-NWs. f) Subsequent RCA and BHF 1% etch of TiN and SiO_2 layers, respectively. g) Magnetron sputtering of 35 nm thick Nickel layer for source/drain silicide junctions. h) Nickel silicidation was conducted at 350 °C for 3 minutes, followed by nitric acid etching to remove residual nickel on the gate metal. i) Spin coating of 180 nm HSQ spacer. j) Diluted HF etching of the spacer (70 nm) and RCA etching of the gate metal were subsequently carried out to enhance the separation between the Gate metal and Source/Drain. k) The spacer was removed and spin-coated once again to maintain the smoothness of the spacer. A laser lithography process was performed to pattern the gate metal. l) HSQ was etched using BHF 1% under the pattered area followed by chlorine based ICP etch to remove the gate metal. m) HSQ spacer was removed and spin-coated one last time to maintain the smoothness of the surface and covers all of samples surface. Tips of the Si-NWs were opened using a diluted HF etch. Gate pads were patterned by EBL with positive resist PMMA-MA/PMMA. HSQ was etched by BHF 1% then the metal deposition was held by magnetron sputtering.

A second oxidation step was employed to form a SiO_2 gate oxide. These steps lead to a residual shared bottom channel thickness of 25 nm and a nanowire pillar diameter of 35 nm. To separate individual transistors, a recess area is created, etching silicon areas down into the BOX. A gate-first approach was chosen to protect the channel and the nanowires from the following process steps. TiN was chosen as the gate metal, and a thin film was deposited using plasma-enhanced atomic layer deposition (ALD). The TiN layer also serves as a diffusion barrier for the following silicidation process in undesired regions and as a selective etch protection layer. In order to achieve isolation between the source/drain and gate metal contacts and to selectively etch different material layers, hydrogen silsesquioxane (HSQ) was employed as a spin-on-glass spacer. When the silicide junctions are created for the source and drain contacts, the nanowires are completely submerged and protected in a 180 nm thick spacer. The spacer, the TiN thin film, and the oxide layer present on the tip of the NWs were then trimmed using subsequent wet etch processes. Following the oxide etch, the sample was immediately placed in the vacuum chamber of a sputtering tool to deposit a layer of nickel. Nickel silicide contacts were created through a rapid thermal annealing process conducted for an adequate duration to ensure the complete consumption of all the nickel. The silicide should be formed in its nickel-rich phase (Ni_2Si) at low temperatures, and the expected length of the silicide is approximately 105 nm. After the silicidation process, the nickel that remained on top of the sample was selectively etched with a wet process, and precisely adjusted to protect all the other layers. To eliminate the possibility of a short circuit from the gate to the source/drain contact and to prevent leakage through the thin spacer layer, the gate metal was once again etched down. Spacer coating and etch back step are repeated to align the gate. A laser lithography process was finally performed to pattern the gate layer and the contact pads.

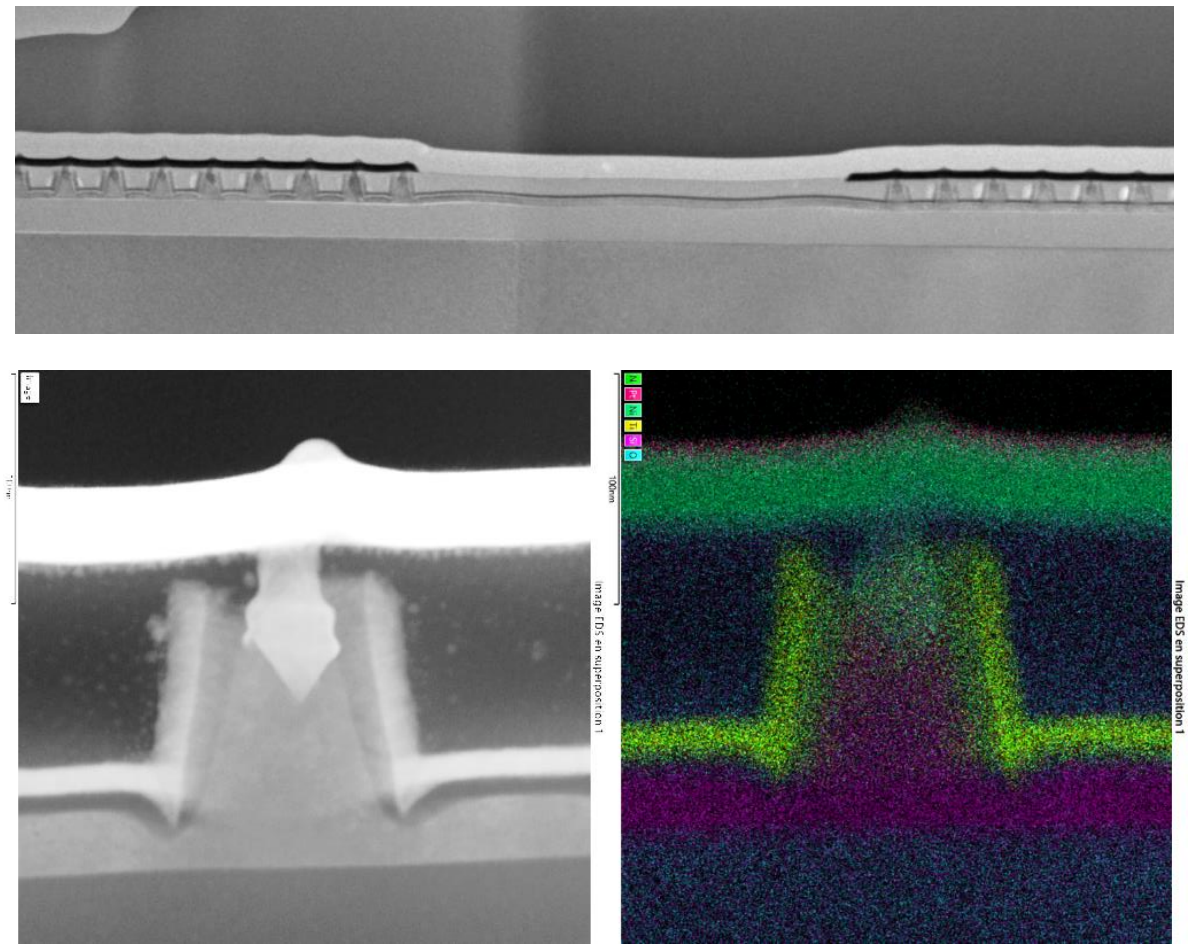

Figure 14. TEM cross sectional views of an ambipolar U-shaped transistor with 81 vertical nanowires at source and drain. a) TEM cross section overniew showing the source and drain vertical nanowire arrays composing the U-Shape b) zoomed-in view of a single nanowire illustrating vertical alignment of the NiSi contact to the TiN gate layer. C) elemental analysis by EDX mapping of the same nanowire shown in b).

II. U-SHAPE TRANSISTOR RESULTS

The process route developed and illustrated beforehand has led to the first-ever experimental realization of U-shape reconfigurable devices. The devices have been characterized structurally and electrically. A cross-sectional image gathered from transmission electron microscopy (TEM) lamella is shown in Fig. 14a. Here, it is possible to observe the two source and drain arrays of 81 nanowires each, as well as the common-channel area between them. An enlarged view of an individual vertical nanowire is visible in Fig. 14b. A clear separation of the source/drain and gate layers is achieved by the vertical HSQ spacer technology. Although the vertical silicon channel shows a more trapezoidal shape, a perfect gate-all-around structure was obtained through the thermal oxide growth followed by the TiN ALD. The gate oxide thickness decreases and align the channel. A TiN spike formation around the vertical nanowire is visible in the common SOI body, most likely due to an over-etch effect. This should be reduced in future iterations to evade reliability concerns. A faceted growth of the vertical nickel silicide is visible, dependent of the crystal orientation of SOI layer. While there are reports that such a structure can enhance the current emission, a flatter interface is assumed to grow with downscaling of the nanowire diameter. An alignment of the silicide to the gate metal around the nanowire is proven, as also illustrated by the elemental distribution in the same single vertical nanowire structure in Fig 14c. Prior to TEM, the same transistor was characterized electrically, and the results are shown in Fig. 15. A drain voltage-dependent ambipolar transfer characteristic is shown in Fig. 15a, featuring pronounced n-type and p-type conduction branches. On the p-branch, an increased gate leakage is measured, most likely due to the TiN spike towards the SOI, but always kept well below the drain's current level. The output characteristic shown in Fig. 15b is shown in dependence of the gate voltage, prooving the Schottky contact formation by it's typical supra-linear features.

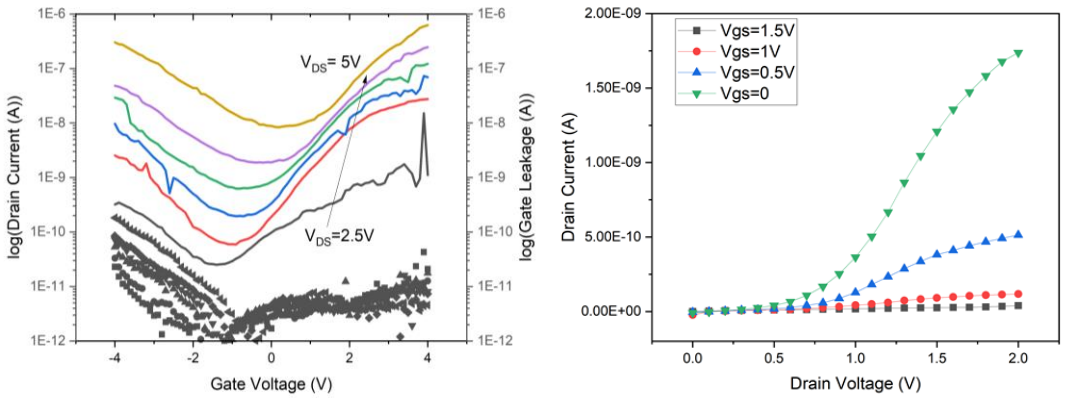

Figure 15. a) transfer characteristics of the U-Shaped vertical ambipolar nanowire transistor, for different drain voltages. Black symbols show the measured leakage currents. b) n-type output characteristic indicating a clear Schottky barrier behaviour.

6. Conclusion

In this deliverable, we described the development of elementary ambipolar nanowire devices in FVLLMONTI. We first reviewed the operation principle and development status of polarity-controllable ambipolar transistors. We then described the detailed strategy how to translate from a purely planar to a true vertical 3D technology in the future. The technological groundwork for this transition was reported here.

In order to achieve the overall aims of FVLLMONTI, this includes a first analysis of RF test structures on FDSOI wafers. Planar RFETs have been built in a GSG pad configuration and delivered to the partners for parameter extraction and compact modeling purposes.

We then described the new concept of common-body RFET, which originates from the unique Schottky barrier-based transport properties. We have experimentally demonstrated how this device can be used for flexible routing of multiple inputs towards a single drain contact. Distinct p- and n-operations have been demonstrated with a high on/off above 10^5. A TCAD-aided study was conducted to elucidate how the novel structure can be transferred to a vertical arrangement, facilitating a U-shape transport.

Finally, a detailed process flow for a U-shape ambipolar transistor design was developed and experimentally demonstrated. Working ambipolar devices have been characterized electrically and by transmission electron microscopy (TEM). Clear Schottky contacts aligned to source/drain gate metal have been achieved in a vertical arrangement. Ambipolar conduction with Schottky-typical output characteristics have been achieved.

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