Project N°: 610456

D5.2a Specification of the interposer

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Abstract:

This deliverable describes the technology options combined with architecture partitioning for the organic interposer of the EUROSERVER HW prototype.

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Confidentiality

Revision history

Version	Author	Notes
1.0	M. HARRAND	Initial version
1.1	D. DUTOIT	Preliminary version
1.2	A. PHILIPPE	Various updates following the decision for a 2.1D integration scheme

Contents

1. Scope

EUROSERVER uses a 2.1D assembly technology where FDSOI28nm-technology chips are interconnected together on an organic interposer by the means of their package inputs/outputs, forming a so-called System-in-Package. This document specifies this complete resulting chip.

2. Package Definition

Four chiplet dies are arranged within a FCTEBGA 40mmx40mm ball grid array package with a full ball matrix of 1 mm pitch (1517 balls). Figure 1 shows the package outline assembly. It has to be noted that with the estimated power consumption of 41W, a heat spreader is required. The substrate would comprise at least ten layers of High Density Interconnect (HDI). The package will be designed with the collaboration of STMicroelectonics.

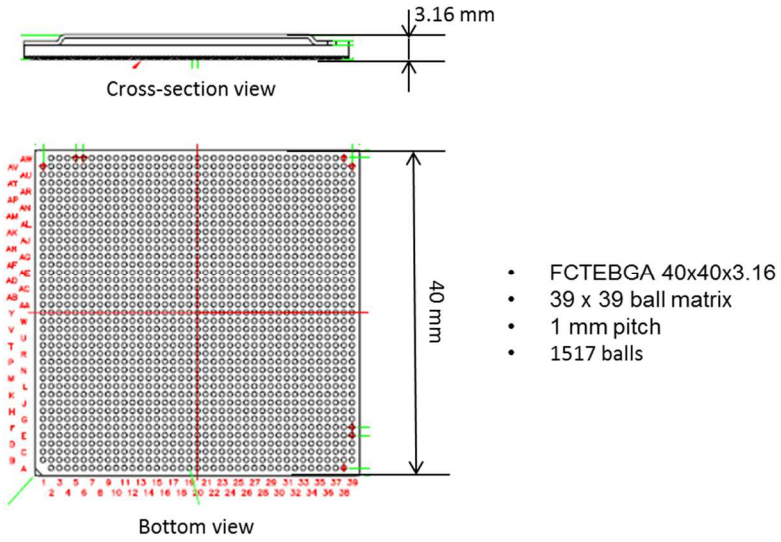

Figure 1. **Package Outline Assembly.**

Figure 2 shows the System-in-Package (SiP) arrangement, its main inputs and outputs, as well as its internal interconnects.

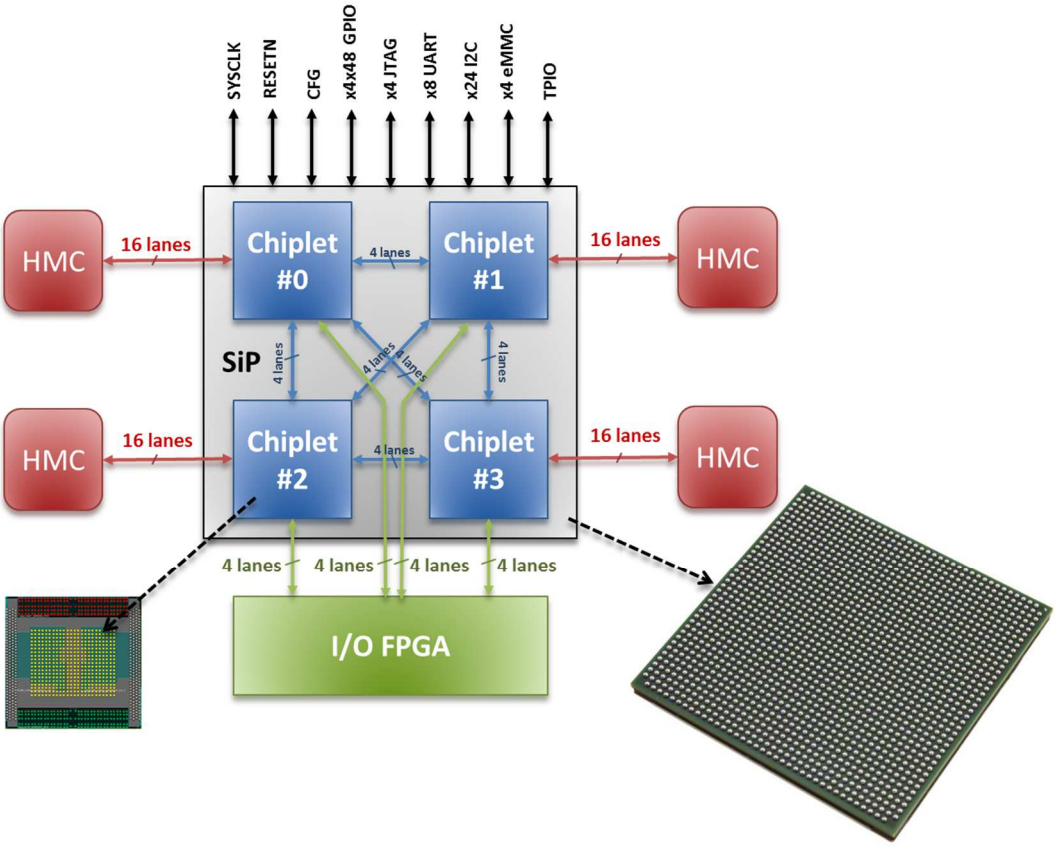

Figure 2. **GAIA2 SiP.**

One can summarize the SiP netlist as follows:

- Four chiplets per package.
- Most of chiplet primary I/Os are propagated outside of the package. For each chiplet:
  - x16 15Gb SR SerDes lanes to HMC device and x4 15Gb SR SerDes lanes to FPGA device,
  - x6 I^2C ports, x2 UART ports, one eMMC and GPIOs,
  - clock, reset, JTAG, trace output port and configuration interface.
- Some of the chiplet primary I/Os are hardwired in the package for:
  - chip-to-chip connections which consist of four S15 lanes per link,
  - Trace chain among chiplets.

Some passive devices are integrated inside the SiP. It is in particular the case for the reference resistor for each S15 SERDES as well as filter capacitor required by each SERDES clock slice. In addition to these, depending on the remaining available space in the package, some decoupling capacitance will be added.

3. Chiplet bump-out description

To enable the connection between the chiplet and the substrate on the front side of the chiplet die, we have peripheral bumps and a central bump matrix. Figure 3 below shows Chiplet layout, as seen from Silicon side.

The peripheral bumps are placed at the edge of the die. The north and south peripheral bumps, which consist of the S15 SerDes I/Os, are arranged in five rows with 160 µm pitch among the rows. The east

and west peripheral bumps, which consist of all standard I/Os, are arranged in five rows with 150 µm pitch. The peripheral bump pitch values represent a good trade-off between the I/O density and substrate traces routing capability among the bumps. The peripheral bumps are used for chiplet signals, for I/O pad supplies and for core supplies. The central matrix has a 200 µm pitch and is used to supply the chiplet core logic with power.

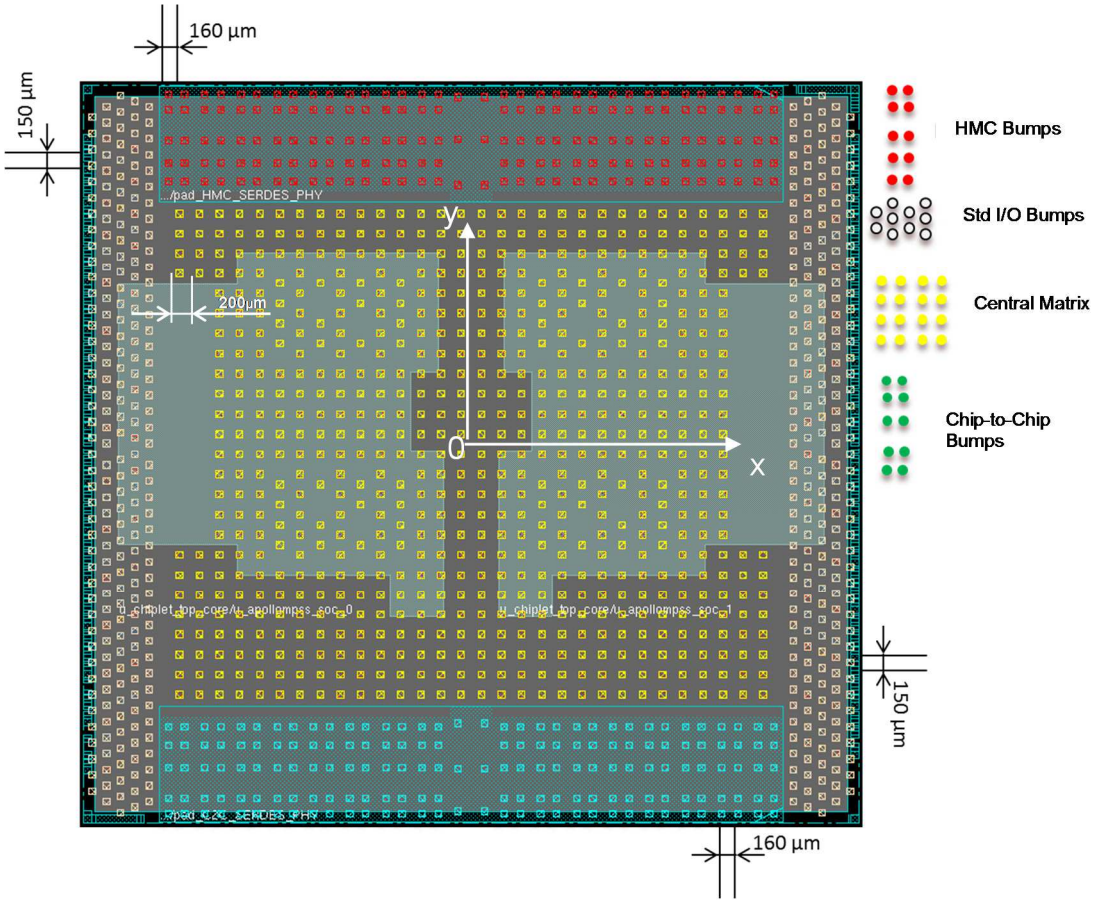

Figure 3. **GAIA2 Bump-out Floorplan.**

The bump technology is solder bumps, fabricated in STMicrolectronics' Crolles facilities, with an Under Bump Metallization (UBM) of 75 µm.

4. System in Package connections

4.1. Overview

The four GAIA dies are placed at 4 corners of a square shape on the package substrate.
There are organized as depicted in Figure 4 below.

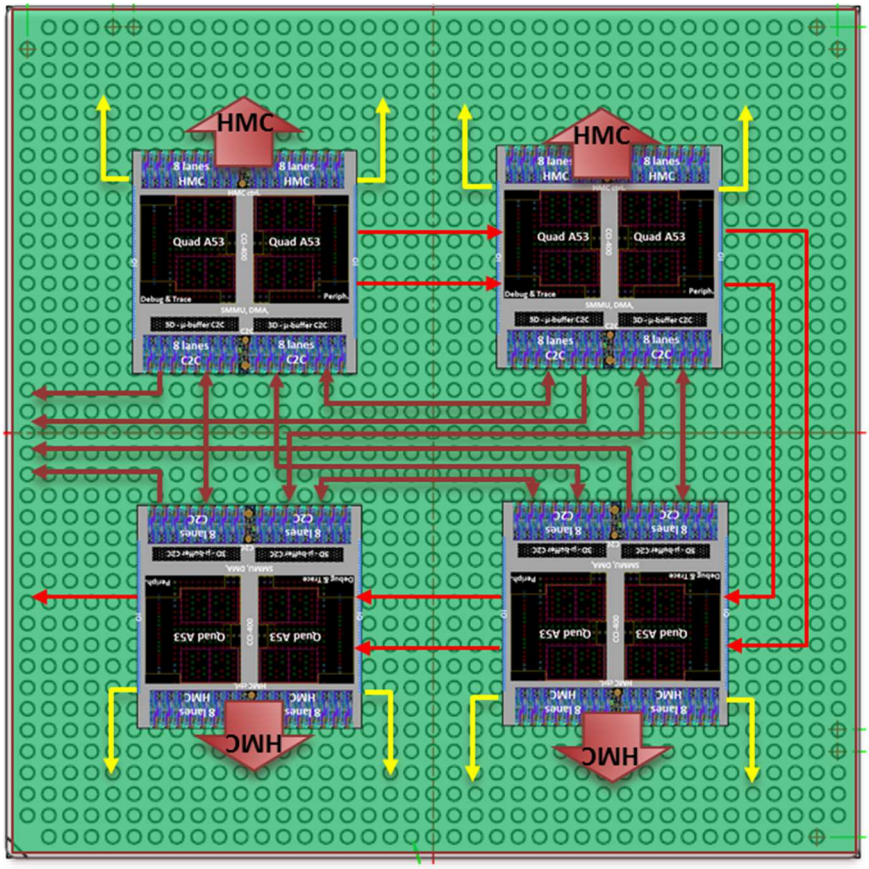

Figure 4. **SiP arrangement.**

4.2. *Connection details*

Figure 5 below gives an overview of the 4 chiplets interconnections within the Package.
Each chiplet has a dedicated HMC memory interface and various I/Os (UART, eMMC, I^2C...) directly connected to the package balls, plus a 4-lane high speed serial link to its neighbors to support inter-chiplet communications.
For software debug purpose, a chained trace bus and a channel for cross trigger information are also bound from chiplet to chiplet.

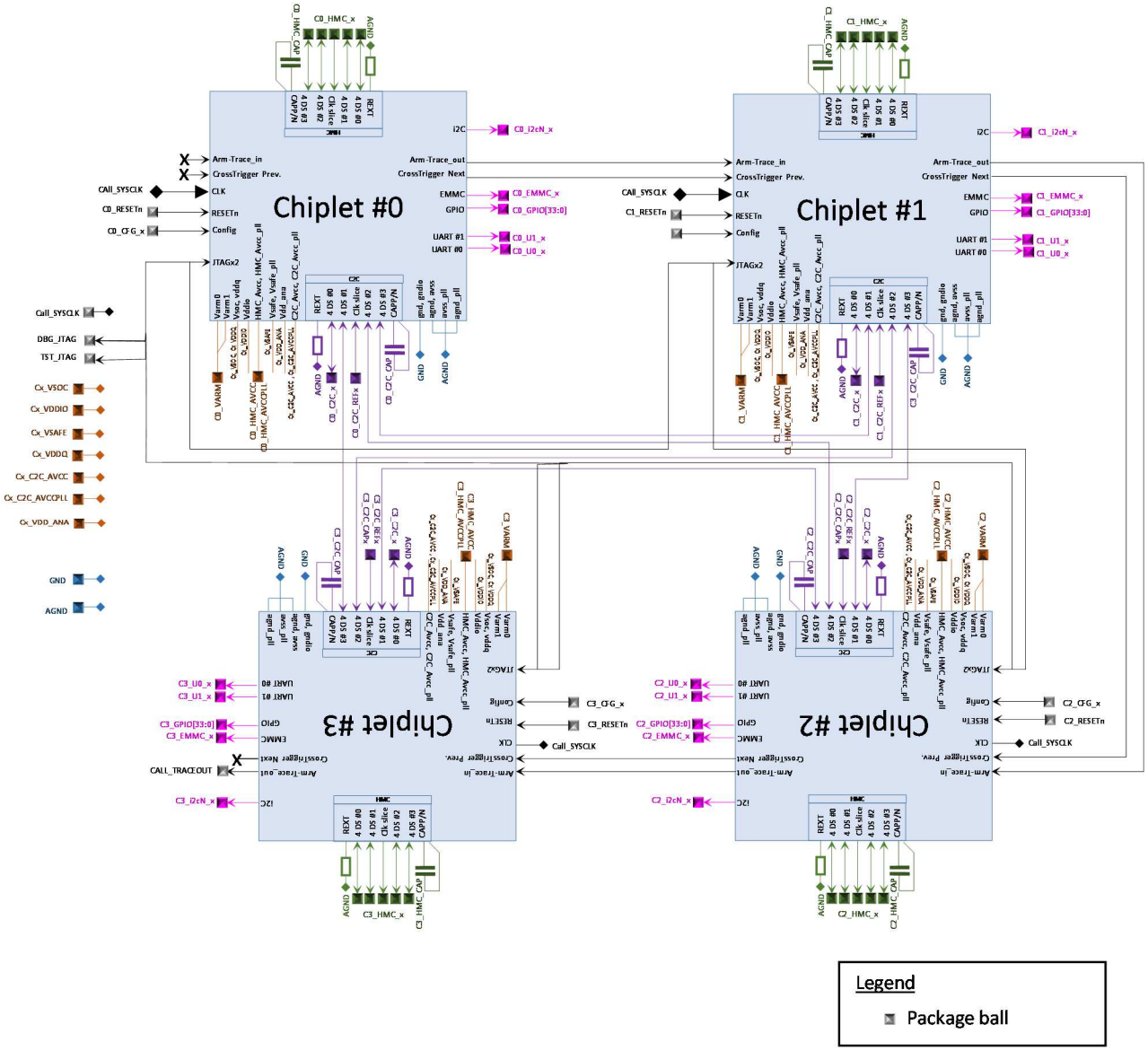

Figure 5. **Connections Details**

4.3. *Power Domains and Grounds*

4.3.1. Ground connection strategy

All digital grounds are connected together at package level.
The analogic grounds are differentiated for noise immunity reason and must be connected at PCB level.

4.3.2. Voltage domain strategy

Concerning the SoC power domains, the preferred strategy is to minimize the number of Power Supplies on the board by connecting the different identical voltage domains of each chiplet to a single power line when feasible. This is the case for Vsoc (1V), Vddq (1V2), Vsafe=Vsafe-pll (1V), Vddio=vio (1V8), Vdd_ana (1V8), AVCC-C2C_serdes (1V), AVCCPLL-C2C_serdes (1V)
Different power lines, per chiplet, have still be kept, for functional reason (one separate VARM CPU voltage control per chiplet) or for noise immunity reason (HMC serdes power supplies).

The System-in-Package ends up with 19 power supplies, as listed below.

4.4. *List of power domains and grounds*

Table 1. lists the power and grounds, their usage and typical values.

Table 1. Voltage domains

Voltage domain	Range	Number in SiP	ball per chiplet	Definition
Ci_Varm	650mv to 1300mv	4	16	CPU voltage domain 1 per chiplet; i in {0,1,2,3}
Vsoc	1V	1	6	Global SoC Voltage domain Shared by all chiplets
Vsafe	900mv	1	2	Always-on voltage domain Shared by all chiplets
Vddio	1V8	1	7	IO voltage domain Shared by all chiplets
Vddq	1V2	1	1	Micro buffer power Shared by all chiplets
Vdd_ana	1V8	1	1	Analog voltage domain (Soc PLLs, ..) Shared by all chiplets
Cx_C2C_AVCC	1V	1	10	Chip-to-Chip SERDES Analog power Shared by all chiplets
Cx_C2C_AVCCPLL	1V	1	1	Chip-to-Chip SERDES PLL Analog power Shared by all chiplets
Cn_HMC_AVCC	1V	4	10	HMC memory SERDES Analog power 1 per chiplet; n in {0,1,2,3}
Cn_HMC_AVCCPLL	1V	4	1	HMC memory SERDES PLL Analog power 1 per chiplet; n in {0,1,2,3}
TOTAL Power domain in SiP		19		

4.5. *Voltage feedbacks*

The system supports DVFS on the CPU supply voltage, at the chiplet granularity. To that purpose, a pair of power feedback pins are defined per chiplet, for voltage level monitoring. They are connected to the Ci_VARM and GND, with i in {0,1,2,3}
See balls couples (H5, H6), (F26, F27), (AP26, AP27) and (AL3, AL4) on ball view picture.

5. Clocks and reset

The System-in-Package implements four asynchronous reset signals, one per chiplet, named Ci_RESETn, with i in {0,1,2,3}. They are not critical in timing.
Clock input of each of the four chiplets is driven by a unique low frequency (< 50MHz) clock signal, called Call_SYSCLK, distributed in the package. This clock drives all the chiplets' PLLs, namely the SoC PLL and each ARM macro PLL.

There are 2 SERDES per chiplet, each of them is driven by a differential Current Mode Logic (CML) reference clock with a 50-ohm termination to AVCC. It makes a total of 16 clock signals (8 differential pairs), namely Cn_C2C_REFCLKN/P, and Cn_HMC_REFCLKN/P, with n in {0,1,2,3}

6. Package Physical details

6.1. Foreseen PCB Organization

The PCB design has not started at the time of writing, allowing only few room for PCB/package co-design during the forthcoming months. However, we tried to anticipate the PCB organization in order to drive the package ball organization in the most appropriate way. Figure 6 gives an overview of the component organization around the Compute Component.

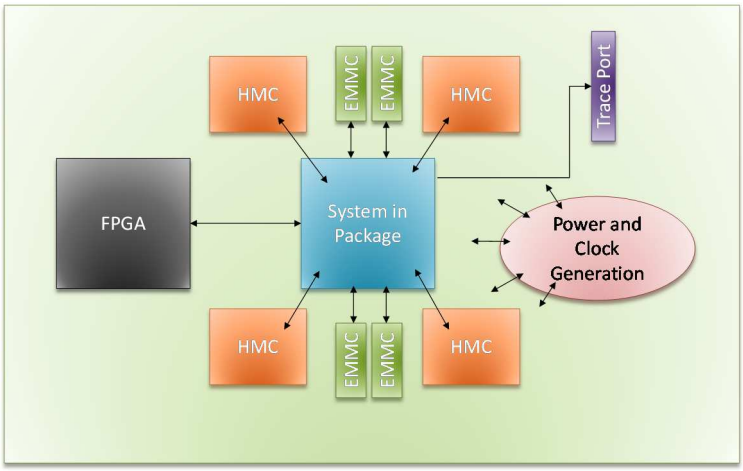

Figure 6. **PCB organization**

6.2. Ball-out

Figure 7 and Figure 8 below depict the EUROSEVER Chip ball-out.
During the ball assignment, priority has been given to the high speed signals, namely all clocks, the HMC interfaces and the Chip-to-FPGA serial link. The 15Gb/s interface signals are distributed on the package periphery with an adequate distance between each other and have associated VSS balls in order minimize the crosstalk phenomenon and ease impedance matching.
The power supply balls are mainly concentrated under the four chiplet dies for a good supply line inductance and to ease the creation of power and ground planes in the package.
The eMMC interfaces are on north and south side of the package, while the GPIOs and other low speed interfaces are concentrated in the center and right side.

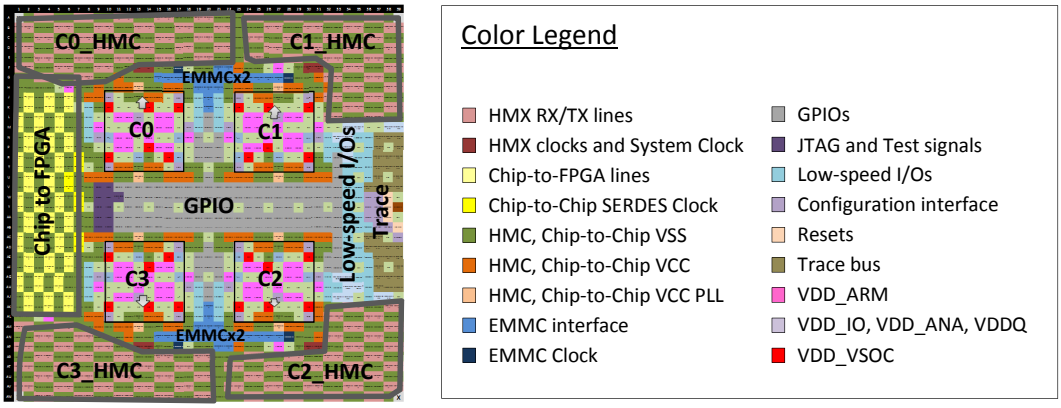

Figure 7. **EUROSERVER Compute node ball out presentation**

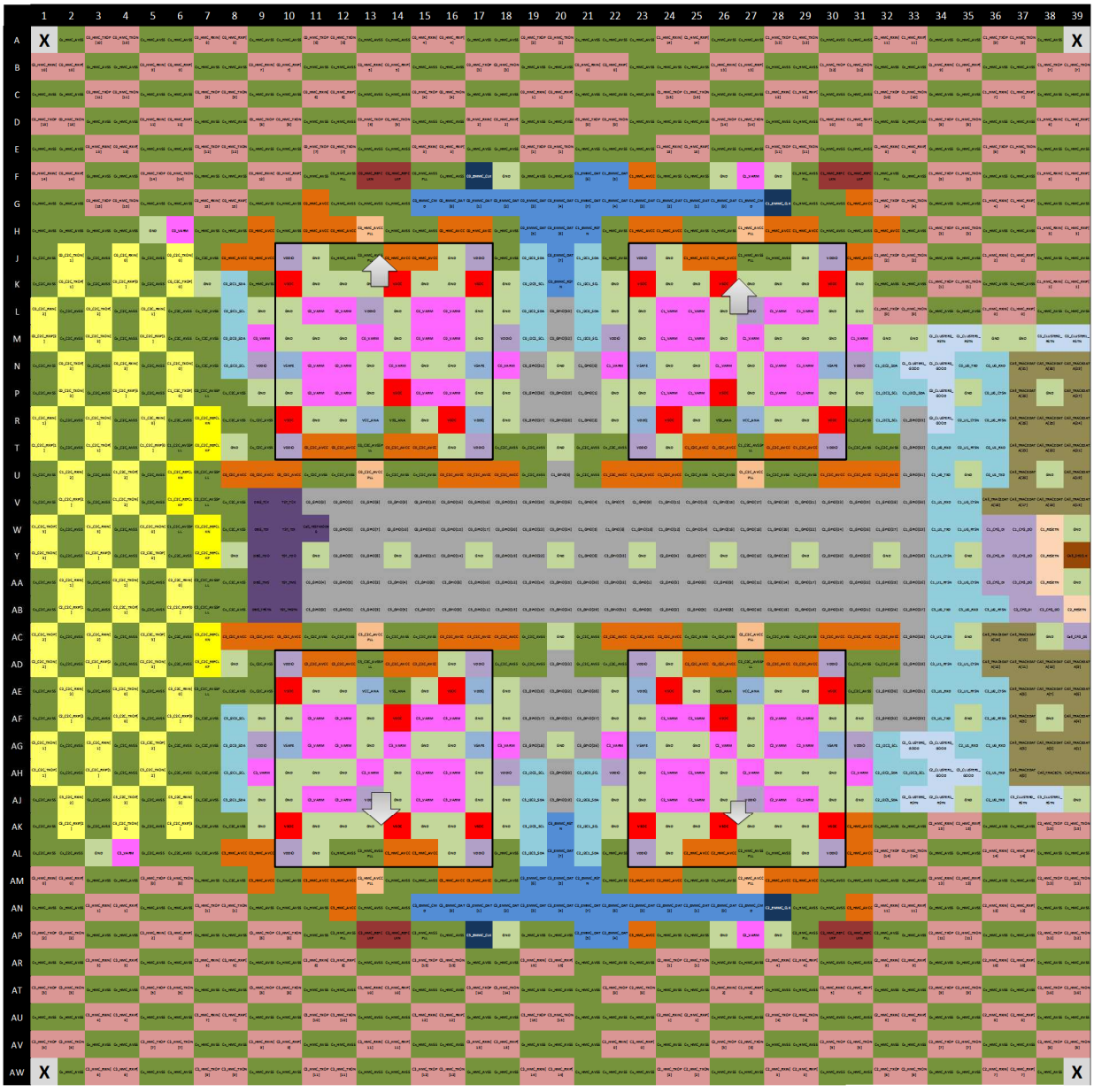

Figure 8. **EUROSERVER Compute node ball out**

7. Conclusion

In addition to the D5.1 deliverable “Chiplet Integration specification”, this D5.2 deliverable “Specification of the interposer” has described the organic interposer that will be used in the EUROSERVER HW Prototype. The System in Package principle is explained and the package netlist is detailed.

Beyond the functional description, the D5.2 deliverable gives some PCB arrangement guidelines and full details of the package ball out, with a specific emphasis made on high speed signals, clocks and power, providing this way all the information required for the EUROSERVER application board design.

END OF DOCUMENT