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Elementary VNWFET devices – JL

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DOCUMENT ABSTRACT

This document describes the optimization of essential building blocks of the FVLLMONTI technology: the elementary JunctionLess (JL) Vertical NanoWires Field-Effect Transistor (VNWFET). These devices are fabricated at LAAS-CNRS for the purpose of providing essential devices to WP2 (parameter extraction) and WP3 (TCAD and compact modelling).

Among vertical transport FET, the LAAS JL-VNWFET technology has the particularity of producing symmetrical S/D access contacts (PtSi), fabricated without any lift-off step with a high reproducibility and versatility. The process is a mix between Top-Down (for NW formation) and Bottom-Up approaches (for the contact stack).

These devices show low access resistance (around 1 kΩ.µm) and DIBL (≈10 mV/V) and near-ideal subthreshold swing (≈74 mV/dec), allowing full control of short-channel effects. Devices presented here have NW diameters between 16 and 50 nm with I_{ON} ranging from 70 to 665 µA/µm below 0.9V.

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LIST OF FIGURES AND TABLES

LIST OF ACRONYMS / GLOSSARY

D: Deliverable
LUT: Look Up Table
M: Month of the project
NN: Neural Network
L: Lead
P: Partner
PU: Public
V: Version
WP: Work Package
VNWFET: Vertical Nanowire Field Effect Transistor
JL: JunctionLess
VN: Vertical Nanowire
LB: Logic Block
PC: Polarity Controllable
NV: Non-Volatile
SG or SGAA: Single Gate (All-Around)
DG or DGAA: Double Gate (All-Around)
EBL: Electron Beam Lithography
RIE: Reactive Ion Etching
SoG: Spin-on Glass, flowable silicon oxide
SS: Subthreshold Swing
DIBL: Drain-Induced Barrier Lowering

Introduction

The goal of WP1 is to fabricate VNWFET technologies from devices to logic blocks (LB) including:

i. elementary VNWFET devices (junctionless, JL and polarity controllable, PC)
ii. VNWFETs with non-volatile (NV) programmability
iii. reconfigurable LB with single gate layer PC VNWFETs
iv. double gate layer VNWFET LB.

This report focuses on the fundamental first step of this WP, which is JunctionLess VNWFET devices (see Table 1 below).

Table 1: Description of delivrables of WP1 and their topics

Label	Quarter	Description	Partners	Type	DL
D1.1	M20- JL M32- PC	Elementary VNWFET devices – JL Elementary VNWFET devices – PC	LAAS, Namlab	DEM	PU
D1.2	M38	Elementary non-volatile ferroelectric VNWFET devices	Namlab, LAAS	DEM	PU
D1.3	M50	Reconfigurable LB using PC-VNWFETs	Namlab, LAAS	DEM	PU
D1.4	M50	LB using stacked JL-VNWFETs up to 2 layers	LAAS, Namlab	DEM	CO

LAAS-CNRS has a strong experience on JL-VNWFET fabrication and meets the technological challenge to integrate more complex structures (Double-Gate, Logic Blocks …). This first step is essential for the coming architectures to be implemented.

In the semiconductor industry, much attention is drawn on Gate-All-Around (GAA) transistors since they are the ultimate version of the existing FinFETs [1]. However, these architectures are often fabricated horizontally [2], which means that they still rely on planar layouts that limits the accessible gate length and source/drain contact area, even for horizontal GAA silicon nanowires that can surpass nano-sheet devices due to their excellent electrical properties [3], [4]. These constraints can however be lifted or relaxed by the vertical integration of gate-all-around nanowires (VGAA-NW) offering several key advantages in terms of processing and circuit design [5]: Firstly, since the gate length (Lg) is defined vertically, it can be relaxed without area penalty, which allows for some latitude in the NW diameter while keeping optimum short-channel-effects control [6], [7]. When scaling down the device, this allows for a better gate controllability compared to planar FETs, lowers the power dissipation and also permits to easily integrate nanowires in higher density arrays [8], [9]. The vertical nanowire platform further provides the possibility of stacking multiple gates along the nanowires, as already demonstrated for vertically stacked NW-FETs [10], [11].

One key issue is the development of reliable multi-level S/D contacts, where each termination can be addressed independently from one device to another, with a high interface quality. A general problem for most experimental vertical devices is the contact fabrication based on lift-off processes, frequently used in small-scale academic processes, which induces organic or metallic contamination during the resist stripping from either the resist itself or the metal layer on top.
More reliable contacts can be obtained by replacing the lift-off process with the etch-back technique that is already well-established in the semiconductor industry. Without the definition of a resist mask, a contact metal layer is directly deposited on the substrate, ensuring a flawless contact interface, and subsequently shaped by removing undesired areas of metallization through selective wet-etching.

Another critical issue that challenges the fabrication of VNWFET is the asymmetry inherent to the vertical approach regarding the S/D contacts. We have generally a bottom contact (base of the NWs) which has quasi-metallic electrical characteristics but contact at the top can be difficult to contact properly and generates high resistance [6], [9], [12], [13]. We developed a self-aligned symmetrical process that allows to create metallic contacts both at the bottom and top of the NWs in a single step.

Finally, in the coming objectives of stacking multiple levels of metal layers to build Logic Blocks and implementing complex architecture, these elementary JL-VNWFETs must present high reproducibility and high yield. Here, we propose and develop for the first time an innovative approach to create high-quality symmetrical contacts based on lift-off free process at wafer scale. By Implementing this new strategy in a rigorous process-flow as close as possible to the industry, we demonstrate a great overall improvement in term of static performance, reproducibility and yield.

The following requirements have been targeted in FVLLMONTI project WP1:

- **Geometry challenges with VNWFET presenting:**
  - 15 to 60 nm channel diameter
  - sub-20 nm gate length
  - nanowire spacing down to 100 nm
  - Large choice of nanowires per device: 1 to 625
- **Electrical performances:**
  - I_{ON} of at least 300 µA/µm at a supply voltage below 0.9V with scaled gate length
  - JL transistors with $I_{ON}/I_{OFF} > 10^5$ at $V_{DD} = 1$ V

Lastly, device configurations should include devices for static characterization (involved in Task 1.5) as well as devices with a dedicated layout (coplanar access for RF probe tips) needed for RF measurements (WP 2)

Large-scale fabrication of vertical gate-all-around nanowire transistors with improved performance

I. FABRICATION PROCESS

Standard JL-GAA-VNWFET fabrication process can be summarized in height elementary steps presented in Figure 1. First a 4'' Si wafer is spin-coated with a 100 nm-thick electro-sensitive flowable oxide which allows high-resolution direct e-beam writing of the desired patterns (resolution down to tenths of nanometers in diameter [14], [15]). After chemical revelation, these negative tone resist patterns are used as a transfer-mask for a RIE step to form Si NWs. Etching conditions are finely tuned to obtain vertical walls, NWs height up to 250 nm (depending on the needs) and smooth surfaces (Fig. 1-I).

Then a standard wet oxidation is performed on the full wafer and selectively etched to drawn the “bottom" contact and access of the device (Fig. 1-II). This step ensures: a) a good dielectric isolation between devices and layers; b) a decrease of roughness and impurities on NW walls; c) an easy way to reduce the diameter of the NWs without being too aggressive in the pattern design. It allows to have more control and reproducibility in the lithography by designing larger NW (typically 40 to 100 nm) and then reduce their diameter down to 15 nm (for the smallest).

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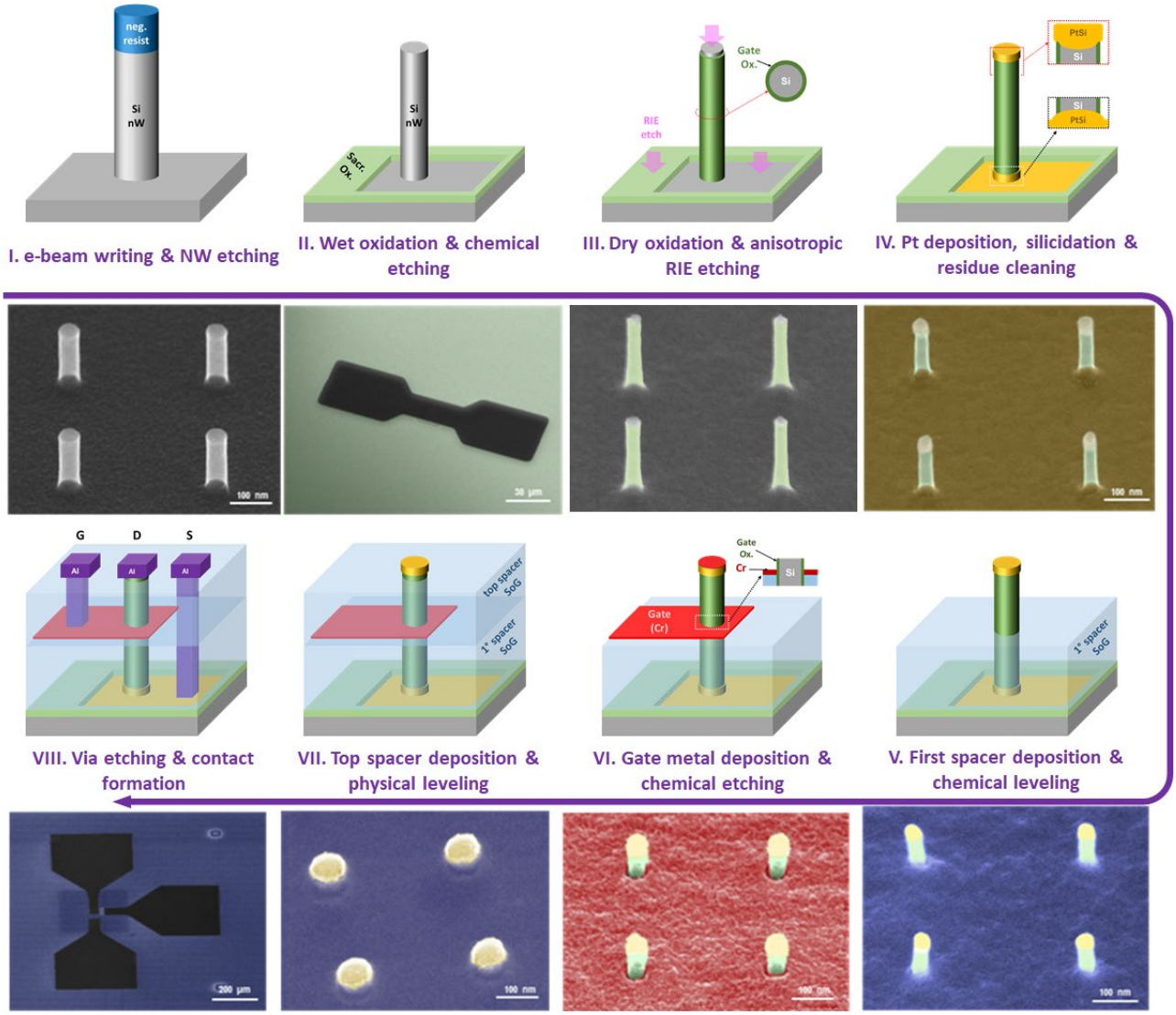

Figure 1: Schematic 3D illustration and tilted SEM image for every step of fabrication flow for JL-VNWFET.

I. Vertical Si NW array obtained by top-down fabrication.
II. Sacrificial oxidation, masking and chemical etching (bottom contact definition & NW shrinking).
III. Gate oxide deposition and RIE etchback definition.
IV. PtSi Source/Drain silicidation.
V. First spacer (Spin-on Glass) deposition and structuration (levelling).
VI. Metal Gate deposition, masking and structuration.
VII. Top spacer (Spin-on Glass) deposition and RIE etching (levelling).
VIII. Vias etching through SoG, Al deposition and contact pads definition

The full wafer gets then a dry oxidation step to grow a gate oxide around the nanowires. This oxide is anisotropically etched in a RIE reactor (Fig. 1-III). This procedure allows to prepare top and bottom contacts of the NWs free of oxide for the following silicidation step while keeping high-quality oxide around the NWs.

PVD Pt is then deposited on the whole wafer and annealed to form PtSi. As this silicide only form in contact with pure Si, oxidized surfaces are not affected and Pt remains in its metallic form. A chemical etching specific to pure Pt removes the remaining metal from unreacted surfaces (NWs walls and SiO_2-protected areas) (Fig. 1-IV).
The bottom PtSi contacts are then isolated from the rest by forming a dielectric spacer (Figure 1-V): Spin-on-Glass (SoG) is spin-coated on the whole device and precisely etched to obtain the right thickness (60 to 120

nm depending on the NWs height). The metal gate (Cr) is then PVD-deposited on the whole surface then chemically back-etched to define the metal layer (Figure 1-VI). Thanks to an anisotropic deposition perpendicular to the surface, Cr will surround the NWs and its thickness will determine the gate length of the FET. A second SiOx layer is spin-coated on the wafer to form the final spacer between gate and top contact levels (Figure 1-VII). This layer is softly etched (RIE) until the PtSi NWs tips come up. remining Cr at the tip is also chemically cleaned. Finally, vias are RIE-etched through the SiOx spacers to contact bottom and gate levels and Al is PVD-deposited. We use again the same etchback technique to define extrinsic contacts (Fig. 1-VIII) without any lift-off.

The quality of the JL-VNW architecture has been explored by HR-TEM/EDX. A schematic representation of the device is shown in Figure 2-a as a reminder. Two NWs are visible in Figure 2-b as seen in a 20° tilted view: image is colorized on the left part to show the GAA metal gate and the tilt allows to see the "hole" in the metal due to the presence of the NW. The left nanowire is analyzed by EDX in Figure 2-c that shows the quality and the symmetry of bottom and top PtSi contacts (in yellow). High-magnification views of the top and bottom interfaces have been taken from the Figure 2-d: abrupt transition can be seen between PtSi and Si (on top (e) and bottom (f) contacts) and oxide is visible surrounding the Si NW: Gate SiO_2 oxide on top and mostly SiOx SoG at the bottom.

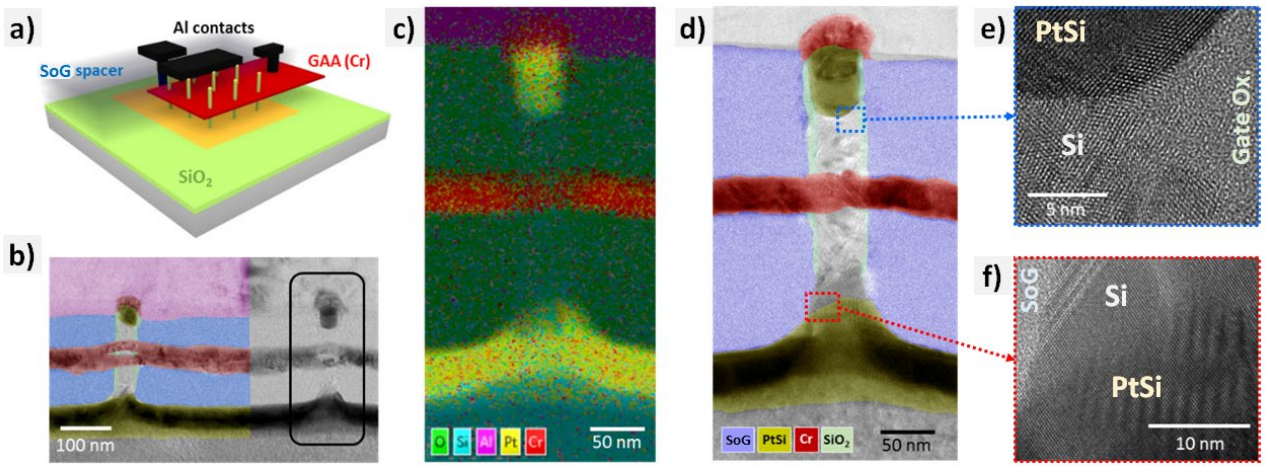

Figure 2: Details on nanowire fabrication quality:

a) Schematic aerial view of a vertical FET device implemented on a dense nanowire array with extrinsic access connecting different levels

b) Partially colorized TEM cross section of the nanowire array in tilted view (20° angle) exhibiting the gate-all-around the nanowires.

c) A single nanowire, framed in (b), has been analyzed by EDX

d) Magnified TEM image has been colorized to show the different layers of the device: the Chromium gate surrounding each nanowire, the symmetrical silicified S/D (PtSi) contacts and low k dielectric spacers (SoG) separating the S/D contacts from the gate

e) High magnification TEM images of the silicide contact interfaces for top contacts.

f) High magnification TEM images of the silicide contact interfaces for bottom contacts.

II. MAIN PARAMETERS / CRITICAL DIMENSIONS

Spacing / Pitch:

Here we demonstrate our ability to fabricate JL-VNWFET devices with spacing (distance between to NW) as low as 100 nm. The challenge here is not only to have a good resolution for the e-beam writing (which is clearly accessible on standard equipment) but also to ensure that the physical RIE is as effective when NWs

are closer to each other and also that the different layers deposition/etching is not affected by these small distances.

In Figure 3, NWs arrays are compared at different stages of the process for 300 nm (top images) or 100 nm (bottom images) spacing. Neither before (a&b) nor after (c to f) SoG spacer deposition any difference can be seen between NWs. Especially when focused on the spacer step – which could be more easily affected by spacing-dependent wettability issues – one can see that SoG surface is flat even at NW proximity. Fully functional devices have also been TEM-prepared to observe the good quality of the final structures either with 300 nm (Figure 3-g) or 100 nm spacing (Figure 3-h).

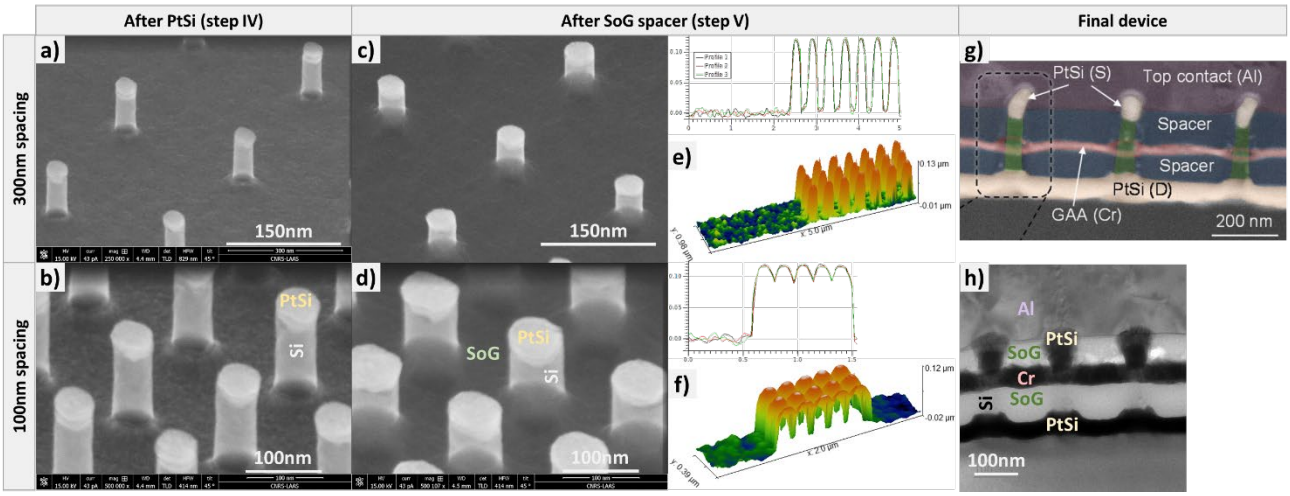

Figure 3: 300 vs 100 nm spacing NWs comparison at different stages of fabrication.

- **a&b)** **SEM tilted images after Pt silicidation**
- **c&d)** **SEM tilted images after first spacer deposition**
- **e&f)** **AFM images after first spacer deposition**
- **g&h)** **TEM cross section images on complete device**

I. DEVICES

A typical chip produced at LAAS-CNRS is presented in Figure 5. The total footprint (pink rectangle) is 7.5 x 8.3 mm² and can contain up to 220 individual structures. We designed them to test various configurations as well as parameters (NWs diameter, spacing…). On a 4'' wafer, 9 chips can be fabricated at the same time.

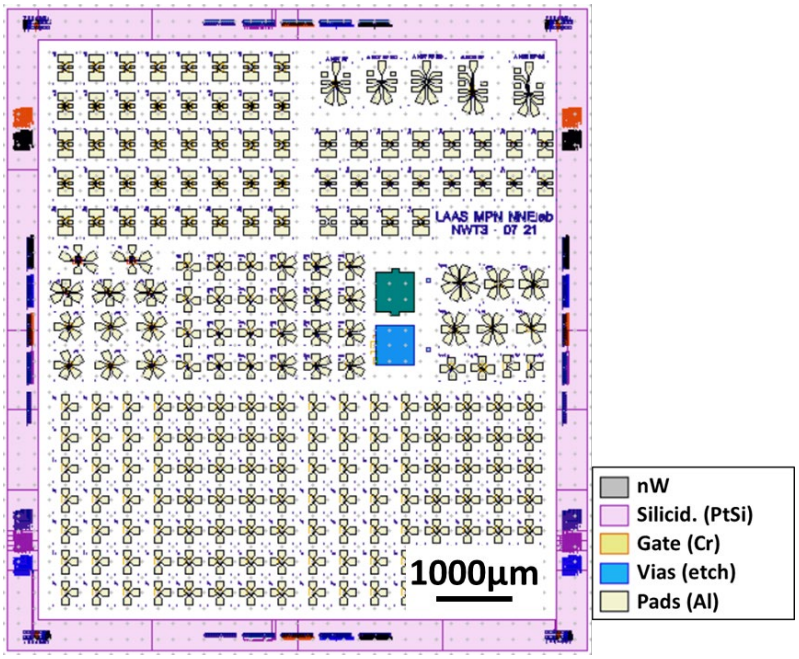

Figure 4: Design example of a full chip produced at LAAS-CNRS.

In Figure 5, two typical JL-VNWFET structures are presented:

- a): a simple transistor for static measurements (close-up view in c)
- b): transistor designed for RF measurements integrating coplanar pads (close-up view in d)

Most of the 200 x 300 µm² surface of the static transistor (Figure 5-a) is taken by the required accessibility of the pads (100 x 100 µm² each) and the active part of the structure is below 60 µm² (around 7.5 x 7.5 µm² for a 10x10 NWs array with a 350 nm pitch) – acknowledging that we designed relaxed structures for research purposes.

RF structures (Figure 5-d) are designed to distribute evenly the electric field with its double source access. Each size of component has its "Open Circuit" (Figure 5-e) and "Short Circuit" (Figure 5-f) counterpart to compensate for the parasitic components during the characterization.

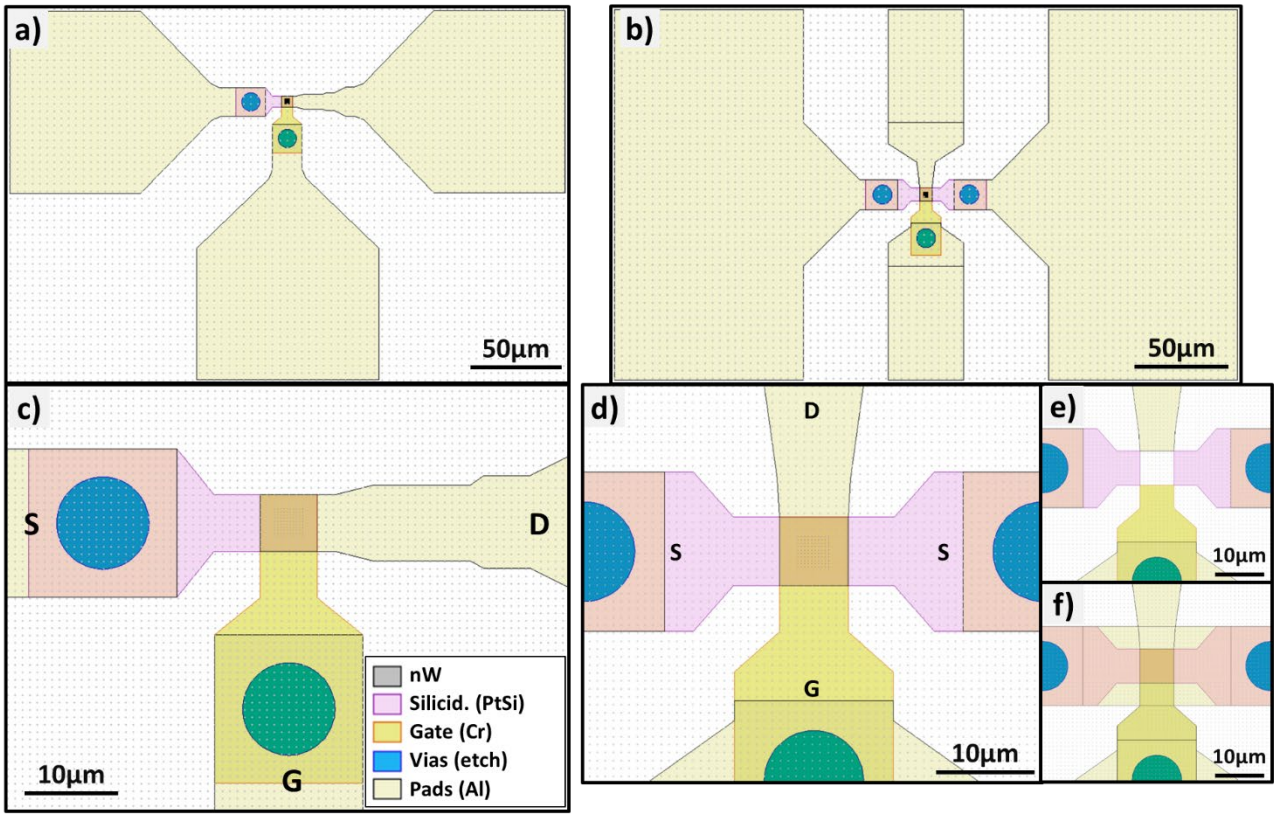

Figure 5: Design of typical JL-VNWFET configurations

a) General overview of a simple FET with 100NWs-array (diameter before oxidation 50 nm, spacing 300 nm) for static measures
b) General overview of a RF FET with 100 NWs-array (diameter before oxidation 50 nm, spacing 300 nm) for dynamic measures
c) extended view of a)
d) extended view of b). This device is complementary with:
e) same device for open circuit compensation
f) same device for short circuit compensation

II. ELECTRICAL CHARACTERIZATION PERFORMED AT LAAS-CNRS

I_D-V_G & I_D-V_D:

Electrical characterizations of such vertical NW architectures with a nominal gate length of 18 nm have been performed with a cascade prober and parametric analyzer "Agilent 4156C". Static characteristics (I_D-V_G and I_D-V_D) at room temperature of NWs array devices with NW diameters ranging from 16 nm to 45 nm are presented in Figure 6 (a to c).

The devices exhibit high drive currents (normalized by the number and the diameter of NWs; at V_{DS} = -1.1V) of 241, 649, 964 µA/µm when the NW diameters are 16 nm, 27 nm, 34 nm respectively. With the increasing NW diameter, the strength of the gate control over the channel is decreasing as depicted by the evolution of the I_{on}/I_{off} ratio. While 16 nm and 27 nm NWs show good gate control with ratios of the order of 6 decades for 16 nm (at V_{DS} = -0.1 V), the electrostatic control of the gate degrades quickly for NW diameters larger than 30 nm and the device cannot be turned off at zero gate bias. The threshold voltage (V_{th}) at the on-set of the linear regime of the I_D-V_G plots is also shifted to positive value of V_G.

As the size of the NWs is reduced, the charge density at the oxide/semiconductor interface is lowered as compared to the bulk conductor, effectively decreasing the conductivity and consequently requiring a larger gate voltage in order to reach the required charge carrier density, shifting V_{th}. The diameter variation also

strongly impacts not only the channel resistance but also the access resistance of the nanowire. It can be depicted with the ON resistance, R_{ON} which includes the spacer resistance, the nanowire section covered by the dielectric spacer and the contact resistance of the PtSi-Si contact interface and extract it from the slope of the I_D-V_D plots at low V_D. Normalized R_{ON} values have been extracted at V_g = -1.6 V and V_D = -0.3 V as 5373.0 Ω.µm, 1236.6 Ω.µm and 902.0 Ω.µm for 16/27/34 nm NW diameters respectively, demonstrating a drastic reduction in the access resistance as both the contact and spacer resistance decrease with an increase in diameter.

To scrutinize the resulting improvement of the R_{ON} values of our novel device fabrication process, which is especially important for smallest NWs, we compare R_{ON} values as extracted from previous devices (presented in [16]) using a conventional lift-off process (Figure 6-d). For previous devices with 18/29/43 nm NW diameters, we find values of 4628.5 Ω.µm, 1546.0 Ω.µm and 1433.0 Ω.µm at V_g = -1.6 V and V_D = -0.3 V. The presented etch-back technique thus provides a 20-40 % reduction in the access resistance, attributed predominantly to an improvement of the contact quality (see also [17]), allowing to achieve higher I_{ON} values except for smallest NWs where geometrical constraints dominated the contact resistance.

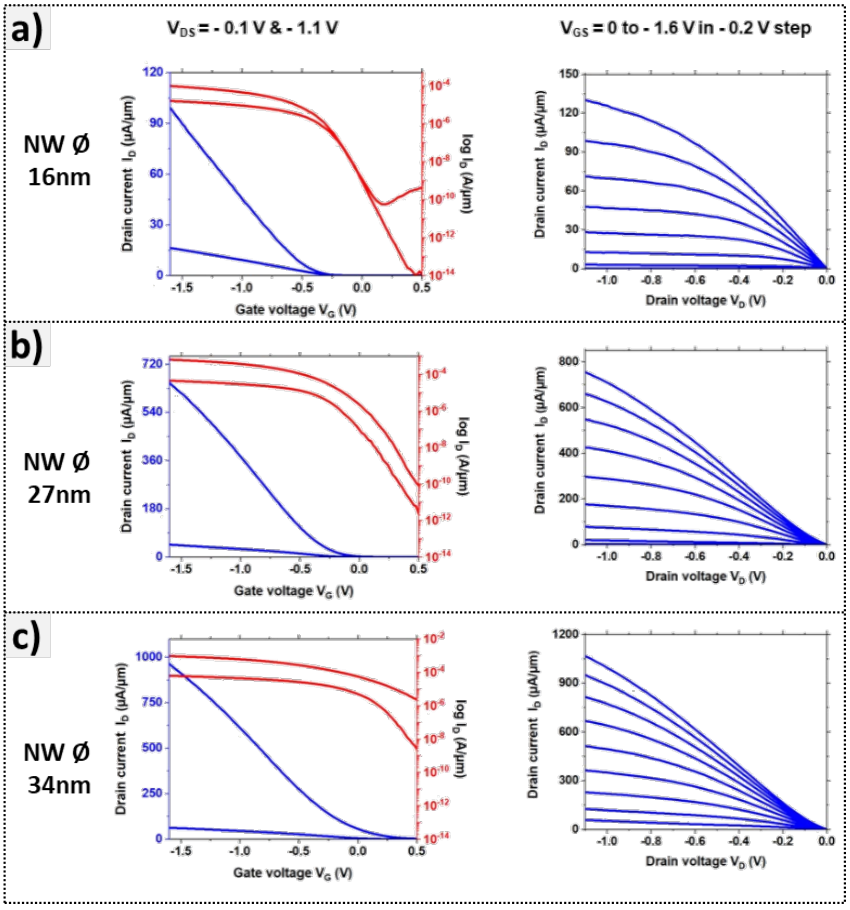

Figure 6: Transfer and output characteristics of JunctionLess GAA p-Type MOSFET on Si:

Physical characteristics (NWs height, doping, etc.) are displayed on Table 2. VNWs have diameters of (a) 16 nm, (b) 27 nm, and (c) 34 nm. Plotted are the drain current over the gate voltage (I_D-V_G) in both linear (blue) and logarithmic scale (red) for different drain voltages as well as the drain current over the drain voltage (I_D-V_D) for varying gate bias.

Table 2: Main characteristics of JL-VNWFET presented in Figure 6

NW diameter	16 nm	27 nm	34 nm
Doping level	$3.5*10^{19}$ cm^{-3}		
NWs height	210 nm		
Gate Ox. Thickness	4 nm		
Gate length	18 nm		
$V_{Th[V\_DS\ -0.1V]}$	-0.1 V	-0.02 V	+0.1 V
$I_{ON[V\_DS\ -0.6V]}$	70 µA/µm	477 µA/µm	665 µA/µm
R_{ON} (Ω.µm)	5373	1237	902
SS	74 mV/dec	87 mV/dec	120 mV/dec
DIBL	10 mV/V	160 mV/V	400 mV/V

SS, DIBL & G_m:

Thanks to the gate-all around configuration, which turns off the device by depleting the doped channel at zero bias, a good immunity against short channel effects (SCEs) is expected. The efficiency of gate control for applied gate bias can be evaluated with the Subthreshold Swing (SS) and the Drain Induced Barrier Lowering (DIBL) as extracted from Figure 7. Subthreshold Swing (left axis on Figure 7-a) is the inverse of the slope in the sub-threshold region (linear regime in logarithmic scale of I_D-V_G) and is linked to the switching speed. The DIBL (right axis on Figure 7-a) is defined as the difference in the threshold voltage V_G when the drain voltage is increased from -0.1V to -1.1 V. It is related to the V_{Th} shift induced by applying voltage on the drain.

At 16 nm diameter, devices exhibit a normally-off behavior at zero bias with quasi-ideal subthreshold characteristics (SS ~74 mV/dec and DIBL ~10 mV/V). The SS and DIBL values plotted in Figure 7-a increase as the NW diameter is increased due to a degradation of electrostatic control while operating under normally-off mode. We observe that even with the very short gate length of the device, SS values can be maintained close to the theoretical value (SS_{th} ~ 60 mV/dec) for VNW-GAA with highly doped substrate, when the diameter of the nanowires is 27 nm or less. In this range of diameters, DIBL also keeps a low value. Above 40 nm the device is strongly perturbed by the short channel effects.

Further, the increase in the drain current with V_{GS} and the device amplification amount can be characterized through the transconductance (G_m), defined by the following relation:

$$G_m = dI_D / dV_{GS} \ | \ V_{DS} = const \qquad (1)$$

Using equation (1), the transconductance for different NW diameters is reported in Figure 7-b, showing a non-linear variation: initially the transconductance increases with the NW diameter, reaching a maximum at around 34 nm (with a value of 675 µS/µm) and then decreases for larger diameters. This can be related with the loss of the electrostatic control for larger nanowire diameters and also reduction of the access resistance. For small nanowire diameters, the access resistance decreases drastically, which in return strongly increases the drive current and thus the transconductance rises. While the access resistance continues to decrease for NW diameters above 30 nm, the impact becomes negligible as the transconductance is negatively affected by the diminishing electrostatic control of the conducting channel, directly decreasing the overall I_{on}/I_{off} ratio of the device. The competition of these two influences leads to the change of the slope in the transconductance, thus peaking at 34 nm, and decreases thereafter. The transconductance thus underlines

the importance of the lowered access resistance through an improved contact quality for the overall performance of the device.

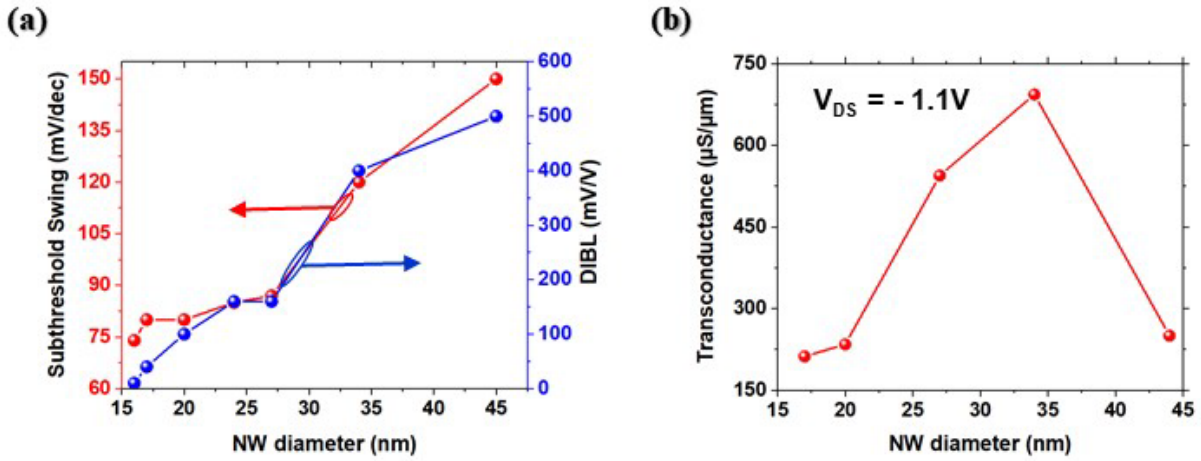

Figure 7: Dependence of the Subthreshold Swing (SS) and DIBL (a) as well as the transconductance G_m (b) as a function of the NW diameter

Influence of the number and spacing of NWs:

As the number and the diameters of the NWs used in our process is of great importance on the electrical performances and available footprint, those parameters have been investigated in Figure 8 through I_{ON} (V_{GS}-V_{Th} = -1 V) at V_{DS} = -0.6 V for NWs diameters ranging from 16 to 34 nm. As expected, the larger the diameter is, the higher the drive current (or transconductance) is measured and it goes the same for the number of nanowires (at a fixed diameter). What is really interesting is the very good linear dependency of these parameters (I_{ON} and G_m) versus the number of NWs that shows that the electrical characteristics can be easily tuned.

This relation shows how reliable and reproducible can our devices be: actually, each individual NW in an array behaves ideally as single transistor connected in parallel to the others. It also proves how homogeneous the access contacts are, thanks to our lift-off free process.

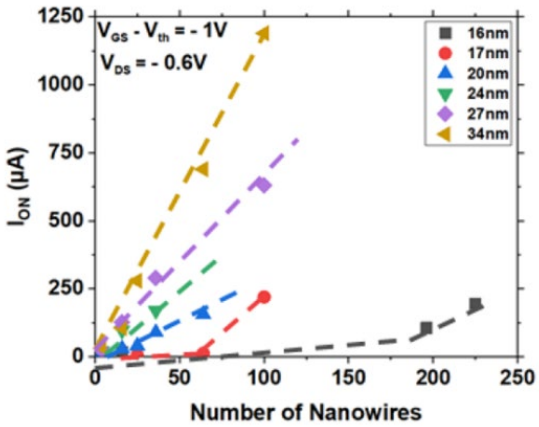

Figure 8: Influence of the number of NWs per device on the I_{ON} at V_{DS} = -0.6V for various diameters.

Figure 9 presents I_{ON} and I_{OFF} versus NW diameter for 16 and 100 NWs arrays where no significant difference can be noted between different spacing. It confirms what has been observed on Figure 3 at the structural level and that our process is perfectly scalable to FVLLMONTI NW density targets without any prejudice on the device performance.

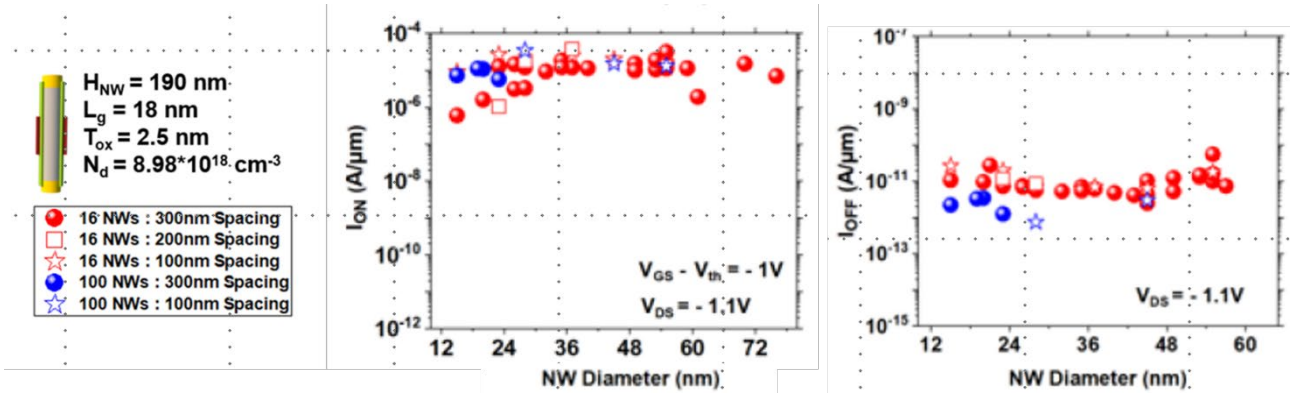

Figure 9: Influence of the diameter on the I_{ON} and I_{OFF} (at V_{DS} = -1.1V) for various spacing between NWs.

Device Yield

The device yield is defined as the ratio between the number of the working transistors at the end of the process to the total number of transistors on the chip. This device yield is closely related to the cost of manufacturing and also determines our ability to stack multiple transistor layer to achieve Logic Blocks fabrication. For 200 nm height NW devices, our yield as to 2021-mid 2022 period has been calculated around 63 ± 1 % on 2 sets of 112 transistors.

This yield is expected to increase since a systematical process-flow analysis has been engaged since mid-2022 to enhance reliability of each individual step.

Conclusion

We demonstrated that LAAS-CNRS is able to provide high-quality JL-VNWFET through an optimized 8-steps process. Nanowires arrays are easily scalable in terms of NW channel diameter (**16 to 45 nm** has been explored here) or NWs/device (**1 to 625 NWs/device**) and showed a great reproducibility due to lift-off free high-quality contacts.

The vertical nanowire approach permits to release constraints on Source/Drain/Gate spacing as well as obtaining very thin gate length easily (**L_g = 18nm** as required). Our JunctionLess approach relies on a one-step symmetrical sillicidation of the source and drain and combined with etchback techniques provide a very good contact quality and access resistance around 1000 Ω.µm (or transconductance below 600 µS/µm) as well as IRDS-compatible Subthreshold slope (**74 to 120mV/dec**).

As a matter of dimension reduction, **100 nm-spacing between NWs has been tested and validated** through structural and electrical analysis.

The Gate-All-Around technology allows a very good electrostatic control (**I_{ON}/I_{OFF} up to 10^6**) meeting the ON/OFF requirements (10^5 at V_{DD} = 1 V). We also confirmed that accessibles I_{ON} are well in the range of the required performances (between **240 to 650 µA/µm** for NWs diameters respectively between 16 and 27 nm).

This new VJLFET generation based on the so-called "lift-off free approach" allow us to reach or overpass the target of the FVLLMONTI project for stand-alone VJL device. The requirements of Milestone 2 (see Table 3) with I_{ON}/I_{OFF} values ten times better than the 10^5 required. The Milestone 8 is also at hand – for JL part – with demonstrators with 16 nm channel diameter, 18nm gate length, 100nm nanowire pitch and Ion/Ioff $_{|Vdd=1V|}$ >10^6.

Thanks to our continuous innovation at the process level, the KPI #4 is also largely reached with typical I_{ON} going up to 513 µA/µm at a supply voltage below 0.9V (0.85V) with scaled gate length (18 nm).

Table 3: Extract of the Schedule of relevant Milestones from DoA Annex 1 part A

Milestone number[18]	Milestone title	Lead beneficiary	Due Date (in months)	Means of verification
MS2	First working JL VNWFET validated	2 - CNRS	14	DC characteristics; Ion/Ioff $_{\|Vdd=1V\|}$ >10^5 achieved for p- type
MS8	Final iteration of elementary VNWFETs devices (JL and PC) validated	2 - CNRS	32	VNWFET demonstrators with 15nm channel diameter, 15nm gate length, 100nm nanowire pitch. JL transistors with Ion/Ioff $_{\|Vdd=1V\|}$ >10^5. PC transistors with Ion/Ioff $_{\|Vdd=2V\|}$ >10^5.

Table 4: Extract of the KPI table from DoA Annex 1 part B

Key performance indicators (KPIs)	State of Art (SOA)	FVLLMONTI	OBJ
KPI4: EDP assessment for JL VNWFETs, I_{ON} of at least 300 µA/µm at a supply voltage below 0.9Vwith scaled gate length	No demonstration for scaled gate and/or p-type device	Scaled dimension and supply voltage with efficient drive current	**OBJ2** MS2 MS4

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