Project N°: 610456

D7.10 Press release highlighting commercial exploitation

March 13th, 2017

Abstract:

This deliverable describes the promotional efforts carried out by EUROSERVER in the final months after the press release detailed in D7.7. A promotional video was created and announced at the HiPEAC conference, at the EUROSERVER workshop in January 2017 at Stockholm, Sweden. An article has been prepared for HiPEACinfo that will be available in Spring 2017. Also a forthcoming press release focusing on the MicroVisor created by OnApp as part of the EUROSERVER efforts is captured.

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The EuroServer Consortium consists of the following partners:

Participant no.	Participant organisation names	short name	Country
1	Commissariat à l'énergie atomique et aux énergies alternatives	CEA	France
2	STMicroelectronics Grenoble 2 SAS	STGNB 2 SAS	France
3	STMicroelectronics Crolles 2 SAS	STM CROLLES	France
4	STMicroelectronics S.A	STMICROELECTRONICS	France
5	ARM Limited	ARM	United Kingdom
~~6~~	~~Eurotech SPA~~	~~EUROTECH~~	~~Italy~~
7	Technische Universitaet Dresden	TUD	Germany
8	Barcelona Supercomputing Center	BSC	Spain
9	Foundation for Research and Technology Hellas	FORTH	Greece
10	Chalmers Tekniska Hoegskola AB	CHALMERS	Sweden
11	ONAPP Limited	ONAPP LiMITED	Gibraltar
12	NEAT S.r.l	NEAT	Italy

Revision history

Version	Author	Notes
0.1	J. Thomson	Initial version created
0.2	BSC	Press release + Magazine article
0.3	J. Thomson	Preparing for review
0.4	J. Thomson	Updated incorrect entries
0.5	M. Gray, J. Thomson	Update to include new ZeroPoint article + update order of Annexes
1.0	J. Thomson	Ready for submission

This document is Public, and was produced under the EUROSERVER project (EC contract 610456).

Contents

1. Introduction

This document outlines the activities related to EUROSERVER press releases. In the final part of the project there have been multiple articles and announcements related to EUROSERVER. We summarise them in this document.

2. Press releases and announcements

In D7.6, the dissemination deliverable we outline all the dissemination and exploitation activities that have been carried out in the scope of the EUROSERVER project. That document does not however capture the two releases and announcements related to EUROSERVER that are contained in this document.

In January 2017, EUROSERVER held a workshop at HiPEAC in Stockholm. In a promotional video (see Figure 1) Paul Carpenter announced the workshop. This was uploaded to YouTube[1] and promoted on BSC's press release channels.

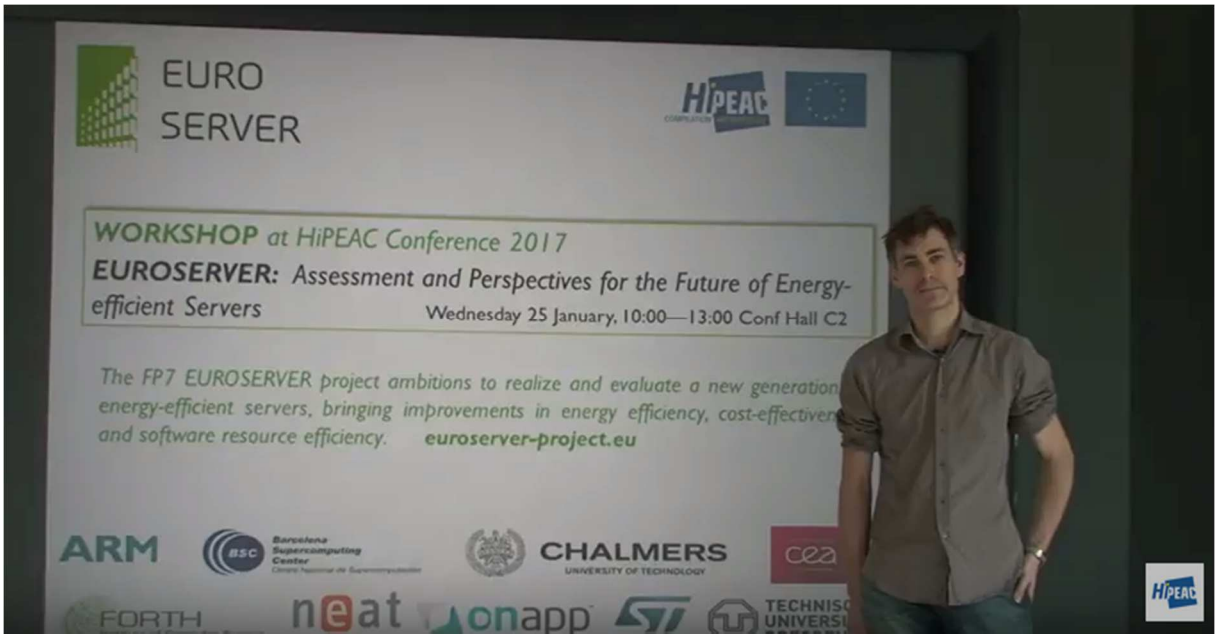

Figure 1: Paul Carpenter of BSC, announces the EUROSERVER workshop to take place at HiPEAC Jan 2017

In addition, in January 2017, CEA with the help of all partners, produced a promotional video for EUROSERVER that has been viewed over 250 times (as of March 2017). It was announced and formally released at the EUROSERVER workshop in HiPEAC. The video is available on YouTube[2] and a screenshot of the video can be seen in Figure 2.

[1] https://www.youtube.com/watch?v=RVFyZUfbSBQ
[2] https://www.youtube.com/watch?v=2EnEKoZ2Tp0

Figure 2: EUROSERVER promotional video

Thanks to the technological innovations which have been delivered by the project, EUROSERVER has received some in-depth press coverage over the last few months, with the two start-ups launched off the back of the project generating the most interest.

In an article of 10th August 2016, *The Next Platform* provided a detailed analysis of the technology produced during EUROSERVER, focusing on Kaleao's plans related to the work carried out in EUROSERVER.

https://www.nextplatform.com/2016/08/10/melding-hyperscale-hpc-reach-exascale/

Meanwhile, *EE Times* showed how ZeroPoint Technologies was a direct result of EUROSERVER in an article of 26 January 2017:

http://www.electronics-eetimes.com/news/memory-compressor-ip-can-save-time-energy-0

ZeroPoint also received interest in Sweden where it is based, where it was covered in a web-article.

http://www.etn.se/index.php/reportage/63280-svenskt-ip-block-foer-ram-komprimering

EUROSERVER was also referenced in an *HPC Wire* article discussing the EU's efforts to fund energy-efficient computing in the EU ICT-05-2017 call for project proposals:

https://www.hpcwire.com/2016/11/11/eu-launches-low-power-chip-effort/

Building on this press interest, in Annex I: we outline a final press release highlighting technology which has not previously been covered, which will be shared with a variety of technical media outlets.

In addition to this press release, we will be publishing an article in the Spring 2017 release of *HiPEAC info*. The text may be found in Annex II:. *HiPEACinfo* is sent to around 600 people, as well as distributed at HiPEAC events and roadshow events. For the spring issue, the HiPEAC event will be Computing Systems Week in Zagreb and the roadshow events will be the Digital Innovation Forum (https://dif2017.org/) and ISC 2017 (http://isc-hpc.com/isc-2017.html). It is also available for download from the HiPEAC website: https://www.hipeac.net/publications/newsletter/

Annex I: Press Release for MicroVisor

MicroVisor, a new hypervisor technology, paves the way for low-power data centres

Grenoble, 13 March 2017. – New hypervisor technology developed as part of EUROSERVER is set to bring significant power savings for data centres. The MicroVisor is a lightweight, remotely controllable and fully configurable virtualization platform that is optimized to operate on all mainstream processors, thus offering a flexible and economical option for data centre architects. By increasing server utilization to unprecedented levels, the MicroVisor helps remove the virtualisation tax typical on cloud service hypervisors, meaning fewer or smaller low power servers are needed and thereby enabling energy savings.

EUROSERVER is a project tasked by the European Commission to develop an energy-efficient server design that can meet the expected demands of exascale computing beyond 2020. The project has developed a range of tools designed to support ARM-based data centres, including the MicroVisor. The MicroVisor has been developed at London-based OnApp, a company specializing in cloud management platforms that has been an integral member of the EUROSERVER consortium.

OnApp's Chief Scientific Officer, Julian Chesterfield, commented: 'We took a Type-1 hypervisor and reduced its footprint. We've taken away the localised controller overhead and created a "clustered hypervisor technology", which means that we can decentralize the control to manage thousands of low power MicroVisor nodes, offering real power savings.'

The MicroVisor works by simplifying how input/output interfaces are presented to virtualization workloads. This multi-tenant system takes a physicalization approach, mapping a virtual storage device onto an underlying ethernet interface resulting in low latency and high performance, which transpose into meaningful reductions in energy consumption.

It is designed to work optimally with UNIMEM, a hardware-assisted memory sharing technology also developed by the EUROSERVER consortium and that allows multiple boards to share physical memory between themselves. Working in unison for optimal power-saving, they allow for better scaling of computer and memory resources, thus paving the way for processor architecture that can cope with the exascale computing workloads that will define the data centre of the future.

The MicroVisor is being released commercially as an integrated system on top of KMAX, an ultra-dense low power ARM-based true-converged server appliance created by KALEAO Ltd. (UK). KALEAO is one of two startups that are bringing to the market technologies investigated in EUROSERVER. Zeropoint Technologies AB (Gothenburg) offers memory compression technologies that have the potential to significantly compress the content of the cache and memory system, with the effect of creating three times more memory.

EUROSERVER, which was coordinated by CEA-Leti (Grenoble) and concluded earlier this year, has made a number of breakthroughs in data centre design, including the prototyping of two platform testbeds: the Juno R2 development board-based system and the UltraScale+, Trenz-powered development platform. Both have energy-efficient quad-core ARM 64-bit Cortex A53 processors, with the Juno also featuring a big.LITTLE design and a Cortex A72 processor. The NEAT designed, EUROSERVER UltraScale+ boards have a Trenz 0808 module and a place-holder for a 32-core ARM System in Package.

Consortium coordinator Isabelle Dor of CEA-Leti concluded: **'**EUROSERVER has delivered wide-ranging energy saving technologies for data centres. Although this project has come to an end, several follow-up projects will take the baton of making the vital steps towards a "European server" that will keep the continent competitive in the ever-changing global ICT marketplace.'

Further information: www.euroserver-project.eu

Project summary film: https://www.youtube.com/watch?v=2EnEKoZ2Tp0

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About OnApp: www.onapp.com
About KALEAO: www.kaleao.com
About ZeroPoint: www.zptcorp.com

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Annex II: Article for HiPEAC Info

Leading data centres into the future: EUROSERVER

Tasked with developing an energy-efficient server design that could be used to meet the demands expected for exascale computing beyond 2020, the EUROSERVER team has concluded the project having produced solutions which could halve the cost of powering data centres and well as greatly increase performance through memory compression.

The project has also led to the development of two spin-off companies; KALEAO Ltd.,headquartered in Cambridge, UK and ZeroPoint Technologies, a startup that has come out of Chalmers University of Technology, Sweden.

But what were the stages that took place behind these impressive outcomes and what new technical knowledge has been gained?

Getting ARM-based microserver designs into the data centre

Consortium partner ARM is a dominant force in the mobile device market where the energy-efficiency and popular instruction set of its processors has led to it being the instruction set of choice for mobile developers. Over the last few years, ARM designed processors have looked to challenge the Intel-dominated data centre market.

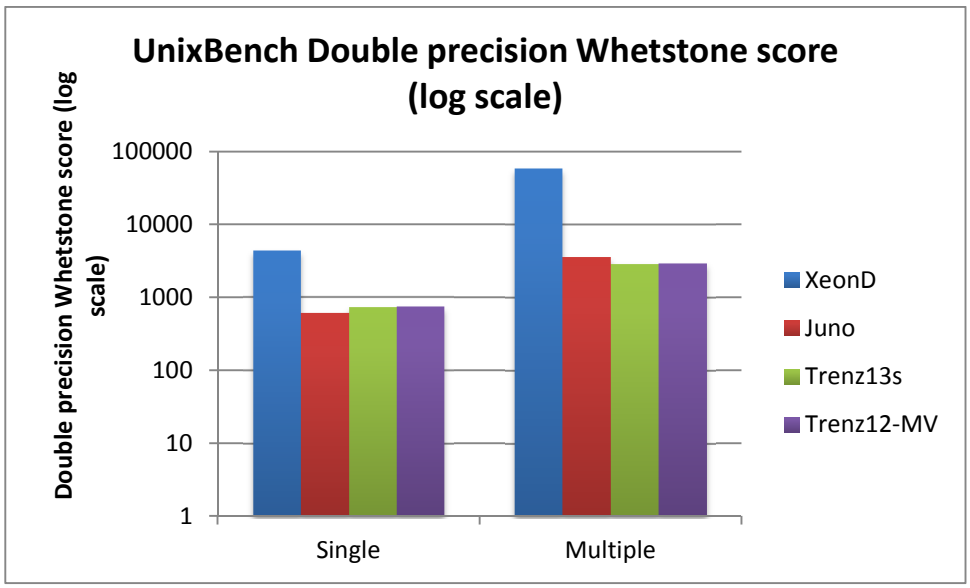
The table below shows the experimental platforms that were investigated. They include a Juno ARM 64-bit development platform, a Trenz board with four energy-efficient Cortex-A53 ARM 64-bit processors and an Intel Xeon D-1540 that we believe is a realistic competitor to ARM in the energy-efficient compute domain.

Table 1: The EUROSERVER platforms that were analysed

	Juno r2 Development Platform	Trenz Development Platform	Intel Xeon D-1540
Cores	2x Cortex-A72 4x Cortex-A53	4x Cortex A53	8x Broadwell cores 16 hw threads
Clock Speed	Cortex-A72 @ 1.2 GHz Cortex-A53 @ 950 MHz	1.2 GHz	2 GHz
L1 Data Cache	48 kB per core	32 kB per core	32 kB per core
L1 Instruction Cache	32 kB per core	32 kB per core	32 kB per core
L2 Cache	2 MB shared	1 MB shared	256 kB per core
L3 Cache	-	-	12 MB
RAM	8 GB DDR3L Dual Channel	4 GB DDR3L Dual Channel	32 GB DDR4 Dual Channel

Some early adopters tried to integrate ARM processors into the data centre but used the ARM 32-bit architecture and hence the idea didn't gain traction. This has all changed with the advent of the 64-bit ARM architecture and, since then, many companies have investigated placing ARM-based micro-server designs into the data centre.

Yet ARM-based processors need to catch up with the large lead-time and massive inertia that Intel has established, the latter having control over the entire ecosystem from design through to fabrication. Intel based processors make up 98% of the data centre market. The scores of typical benchmarks, such as UnixBench, suggest that Intel solutions are at least one order of magnitude more capable than the ARM based solutions that are trying to compete with them, as shown in 3. Where EUROSERVER came in was to develop a server design that benefited from ARM's power-efficiency and addresses some of its shortcomings so as to create a viable alternative to Intel based solutions.

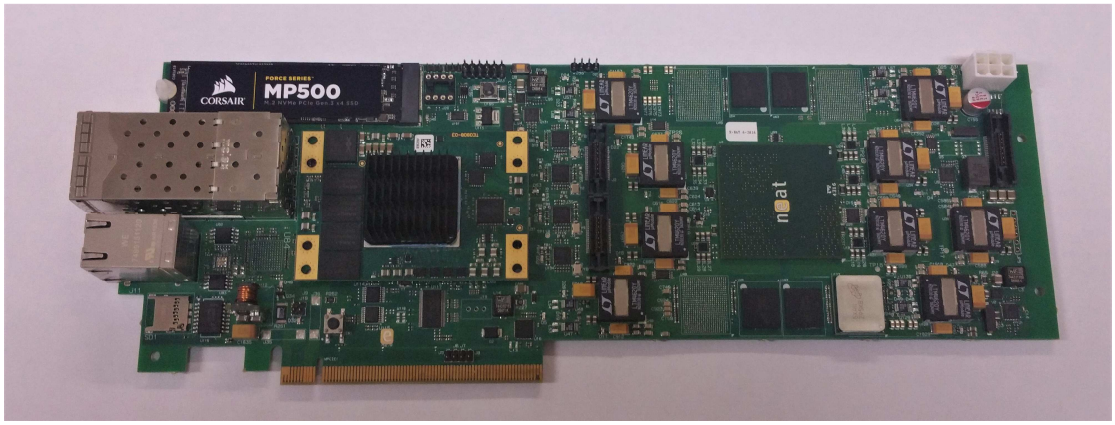


3: UnixBench, Whetstone test results for various devices under test (log scale)

Hardware advances

Over the course of the project, a combination of hardware and software techniques were developed. On the hardware side, two prototype platform testbeds were created; a Juno R2 development board based system and a Trenz development platform. Both have energy-efficient, quad-core ARM 64-bit Cortex A53 processors, with the Juno differing in that it is also a big.LITTLE design and has a Cortex-A72.

The Trenz 0808-based, UltraScale+ system, seen in figure 2, combines a Trenz module with 4x A53 cores with a placeholder for a System-In-Package (SIP) 32-core A53. At the time of writing, the 32-core SIP is not ready but will be included in one of the follow-up projects that has resulted from EUROSERVER, including ExaNeSt, ExaNoDe and EcoScale.



4: The EUROSERVER designed, NEAT produced, prototype board. Not shown are a Trenz 0808 module and a SIP

Software breakthroughs

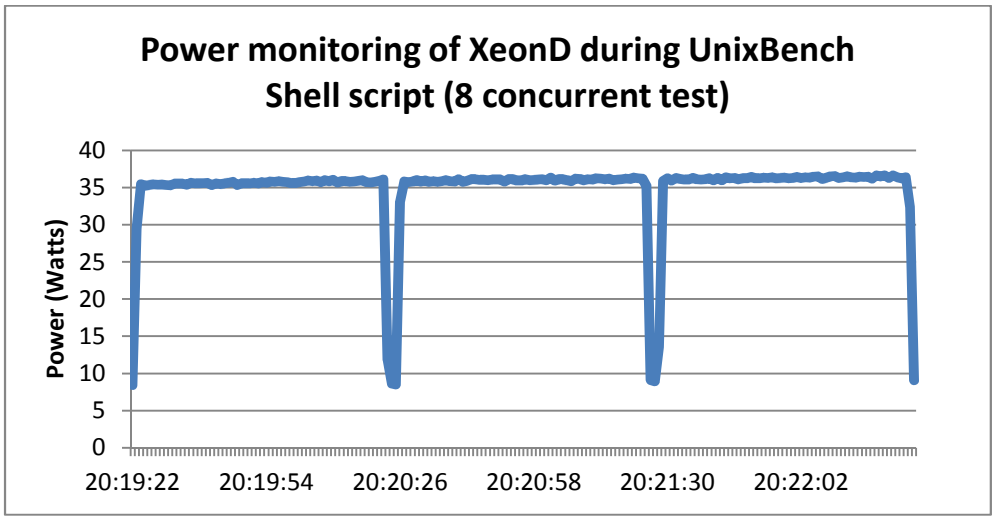
Processor manufacturers in recent years have been limited in how far the frequency envelope can be pushed due to power density, which has led to the rise of multicore chips. EUROSERVER has taken on board this change in design and has developed new scalable technologies, UNIMEM and the MicroVisor, that allow better scaling of compute and memory resources. These will be able to deal better with the exascale computing workloads that are expected in future data centres.

UNIMEM and the MicroVisor represent the project's main achievements on the software side. UNIMEM is a shared memory technology that allows multiple boards to share memory regions between them. This allows for better provisioning strategies and for greater in-memory workloads than are possible with current best-of-breed solutions. Memory from each board is divided into a local and a remotely addressable region. UNIMEM technology is a licensed IP technology and has been investigated by a number of companies and research organisations.

The MicroVisor is a new hypervisor technology that derives from Xen. It is purpose made for low-power, energy-efficient platforms such as ARM that have many, albeit weaker cores. Traditional hypervisors are now quite 'bloated' and require a large amount of resources that are not available to ARM-based boards. Instead a lighter, more efficient platform has been developed that works natively with ARM and Intel architectures. The overhead for workloads running in virtual machines is near negligible, as seen in figure 1.

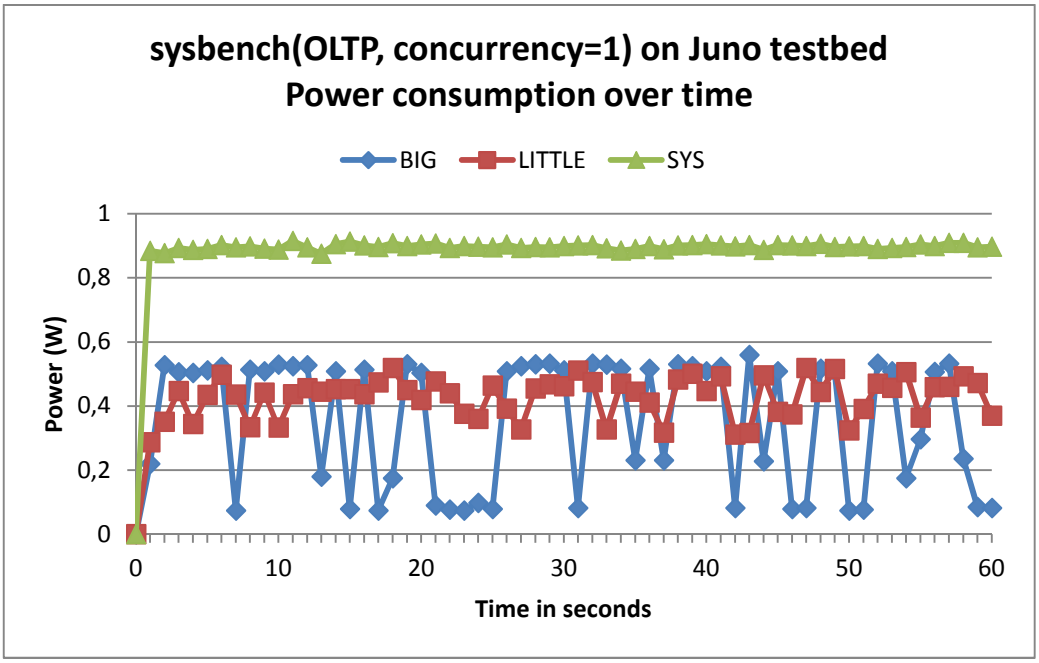
Energy-efficient platforms

Power monitoring techniques such as RAPL are used to expose the power utilized by the XeonD platform to be able to identify the power used by the processor during stages of a workload (see figure 3).



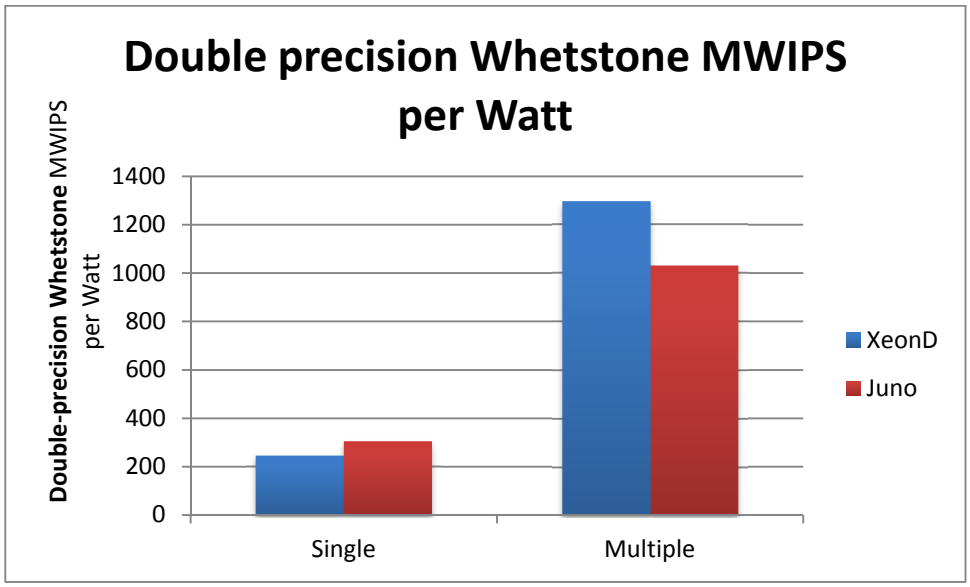
5: Power monitoring of the Intel XeonD while running a UnixBench Shell script test

The equivalent power monitoring has been exposed through kernel modules in the Juno platform to allow monitoring of the ARM system whilst running workloads (see figure 4).

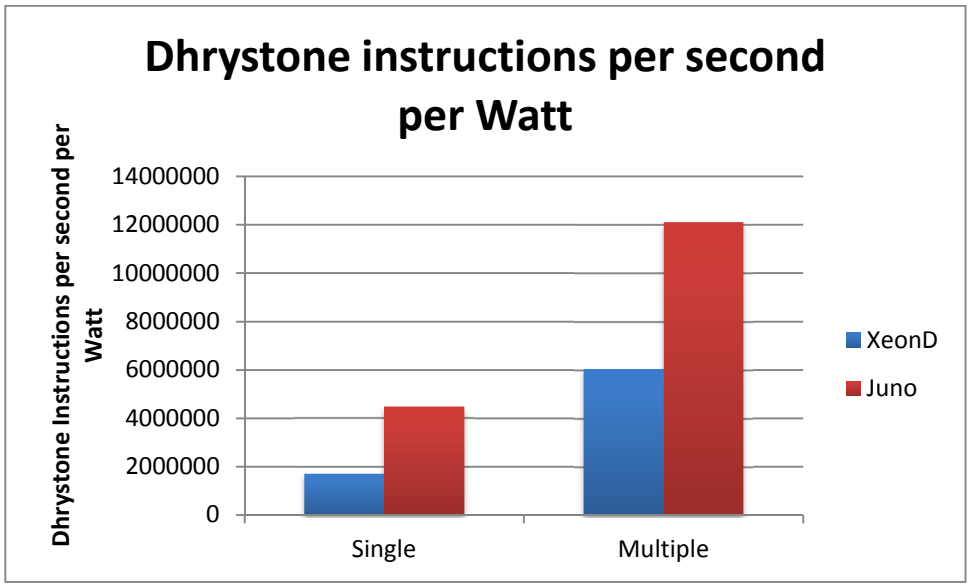


6: Power monitoring of the Juno R1 development board, whilst running SysBench OLTP workload

By looking at the power profile of the devices while investigating the workloads it is then possible to identify the power-efficiency of the platforms - as seen in figures 5 and 6. The power efficiency of the Juno platform shows that, although the ARM-based designs lag behind in raw performance values, they are more energy-efficient and will have a place in the data centre of the future.



7: These energy efficiencies were calculated by taking the Whetstone score and dividing by the average power usage recorded for the processor during this test



8: These energy efficiency values were calculated by taking the Dhrystone scores and then dividing by the average power usage during this test

The final EUROSERVER platform (see figure 7) combines a pair of UltraScale+ boards on a backplane that provides electrical and physical connectivity. These boards will be used in the several follow-up projects to form the basis of a 'European server', a server designed and built in the EU that will keep the continent competitive in the ever-changing global ICT market .

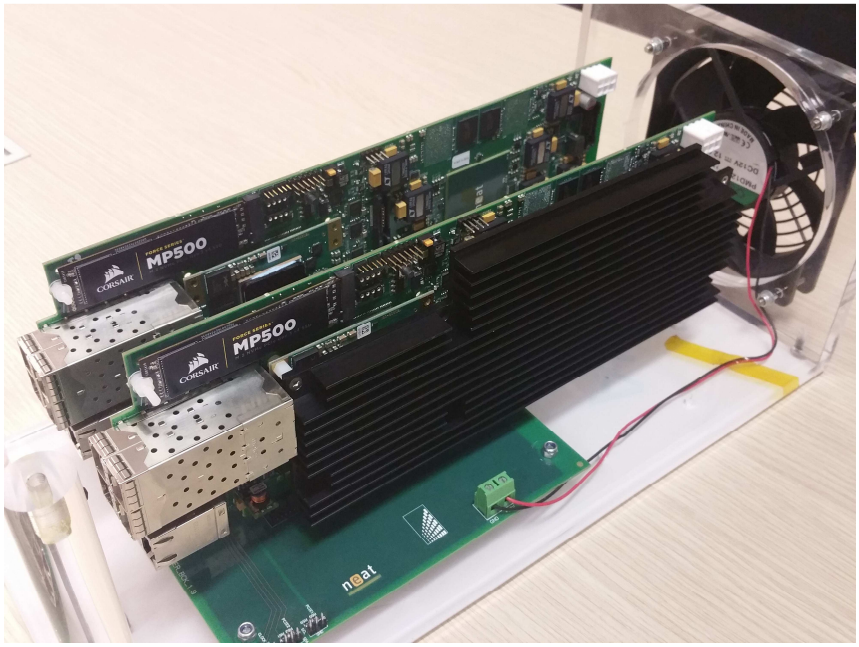


Figure 9: A pair of EUROSERVER boards, assembled onto a backplane with electrical connectivity, designed by EUROSERVER and produced by NEAT

The EUROSERVER consortium was led by CEA-Leti and had as partners ONAPP, FORTH, BSC, TUD, STM, NEAT, CHALMERS and ARM. The project started in September 2013 and concluded at the end of January 2017 and was received funding from the European Union's FP7 programme under grant agreement no. 610456.