Press release

Date	Publication	Content	Reference
Mar 2014	PanEuropean Networks "Science and technology" issue 10	Paragraph "green computing node" about EUROSERVER	http://www.paneuropeannetworks.com/ST10/
Mar 28, 2014	Press release	Europe invests realising next-generation green computing for micro-servers and scalable compute	Spanish press release
Oct 2014	EEtimes	Article on the HiPEAC microservers session and thus EuroSERVER project	http://www.eetimes.com/author.asp?section_id=36&doc_id=1324294
Jan 2015	EEtimes	European server project promotes ARM on FDSOI	http://www.electronics-eetimes.com/en/european-server-project-promotes-arm-on-fdsoi.html?cmp_id=7&news_id=222923411&page=0
Sum 2015	HiPEAC newsletter	Socket over RDMA and shared peripherals for ARM microservers	http://www.hipeac.net/assets/public/publications/newsletter/hipeacinfo43.pdf

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http://www.eetimes.com/author.asp?section_id=36&doc_id=1324294&page_number=1

Microservers Brew in Europe's Labs

At least four microserver projects are brewing in European labs, testing out a variety of processor, system, and software architectures, one researcher reports.

A handful of major microserver projects, mainly funded by the European Union, presented data center servers based on energy-efficient embedded processors at the recent HiPEAC EU Network of Excellence event.

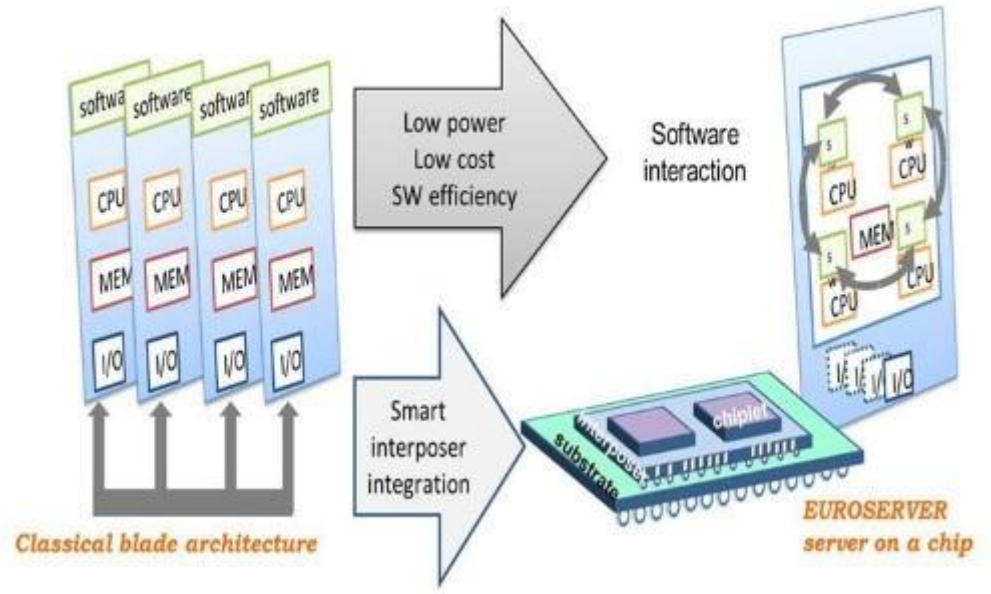
The NanoStreams project brings together European expertise in embedded systems design and high-performance computing (HPC) software to address the challenge of real-time analytics on fast data streams. NanoStreams uses an architecture and software stack that address the unique challenges of hybrid transactional-analytical workloads, encountered by emerging applications of real-time big-data analytics.

The NanoStreams processor is an amalgam of RISC cores and nano-cores, a new class of programmable, custom accelerators. Novel automatic compiler generation and parameterisation technology enables low-effort programming and integration of nano-cores into application-specific, many-core accelerators.

The project's proposed heterogeneous Analytics-on-Chip processor forms the backbone of the NanoStreams microserver. The system also leverages a hybrid DRAM-PCRAM memory system and a non-cache-coherent, scale-out architecture to achieve extreme energy-efficiency. It systems uses a mix of Calxeda SoC and Xilinx Zinq boards.

NanoStreams brings together a consortium of two academic institutions and three technology providers working in partnership with IBM and Credit Suisse. The main advantage of Nanostreams is that it is driven by the needs of real financial workloads and the proposed architecture is evaluated using real stock-exchange data.

In his talk on the project, Dimitrios Nikolopoulos, a professor and research director at Queen's University of Belfast, compared commodity x86 servers and microservers based on the Boston Viridis platform. He emphasized the need for fair comparisons of power consumption not only between the processors but between whole systems including the power supplies, storage and memory subsystems.



The Euroserver uses a processor on a 2.5-D chip stack with an interposer.

The Euroserver project applies state-of-the-art low-power ARM processors in a new server architecture that uses 3D "chiplets." The approach aims to reduce the acquisition cost of the system and scale the numbers of cores, memory capacity and I/O bandwidth it provides. New systems software supports both legacy and advanced features including system-wide virtualization to further reduce energy consumption.

The project takes a novel software approach of managing server resources as multiple coherent islands. It isolates and protects the multiple workloads from each other when they use shared server resources such as I/O, storage, memory, and interconnects. The main advantage of the architecture is it gives the user the option to move tasks and processes close to data instead of moving data around.

The Euroserver consortium includes ARM, STMicroelectronics, Eurotech, and OnApp, in addition to five academic institutions including CEA and FORTH.

EE-Times Europe

http://www.electronics-eetimes.com/en/european-server-project-promotes-arm-on-fdsoi.html?cmp_id=7&news_id=222923411&page=0

A collaborative European microserver project has teamed processor IP licensor ARM and chipmaker STMicroelectronics up with a number of academic and commercial computer and software specialists to try and make technical progress in microservers.

The three-year project, which started September 2013, is expected to deliver an innovative scalable computer system architecture this year and a hardware-software prototype implementation by the end of 2015.

The rise of cloud-enabled smart devices, cloud-based client services and the Internet of Things (IoT) is expected to create an opportunity as they will drive a shift in the needs of the IT infrastructure which is already under pressure to reduce power consumption even as it tries to scale up to serve increasing numbers of applications.

The Euroserver project is advocating the use of low-power ARM processors in a server architecture that uses 3D integration to scale processors, memory and I/O, all managed by system-wide virtualization and efficient use of resources by cloud applications. The group is aiming for a factor of ten improvement in energy efficiency over traditional server and microserver architectures.

Microservers are typically servers designed to serve applications that don't individually require high levels of computing performance but that may have to be done in large numbers and or may have critical latency aspects to performance. In the past servers tended to aim at ever higher performance and in recent years were the almost exclusive domain of the x86 processor architecture of Intel. Lower power microservers are now expected to take up an increasingly diverse number of data handling opportunities. And microservers have long been the chosen ground on which ARM has chosen to fight Intel in data center

John Goodacre, director of technology and systems at ARM and a visiting professor of computer architectures at the University of Manchester, said that the groups collaborating in Euroserver reflect the microserver profile. "TU Dresden is interested in the handling of databases in embedded telecom. Eurotech is a systems company looking at more deeply

embedded applications," said Professor Goodacre. He also noted that that Spain's Barcelona Supercomputing Center is present which reflects an interest in scaling up to take on high performance computing.

Next: The unit of compute

The Euroserver project is leveraging the availability of an octa-core processor chip that ST makes on its FDSOI manufacturing process and also sees importance in using the latest 3D manufacturing techniques, courtesy of project participant CEA-Leti to build the best power-performance trade off it can. "We've tried to take a holistic view of the challenge. It's a mixture of both hardware and software," said Professor Goodacre.

Unit of compute, move the task

One of the foundation stones of the Euroserver project is an idea that Professor Goodacre laid out in a keynote speech at the DATE conference in 2013 – the 'Unit of Compute.'

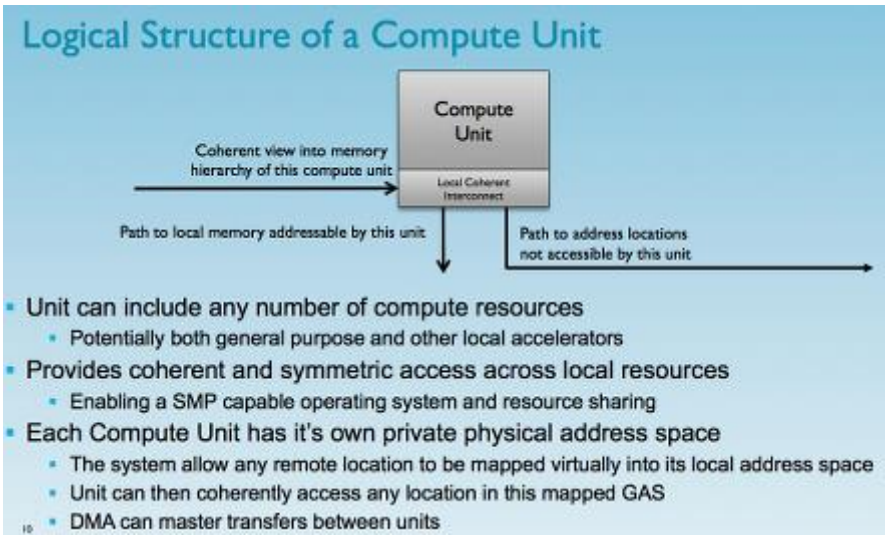


Figure 1: Unit of Compute. Source: ARM

This is the idea of what is the minimum requirement within a computer node to allow its memory to be used by the outside world coherently with a minimum of overhead. A 'unit of compute' is managed by a single symmetric multiprocessing (SMP) operating system within a coherent region of memory. It has a processor system – from one to many cores – local memory, provides a coherent view of its memory to the outside world and has a path to access remote memory attached to other 'units of compute.'

The net result allows the simplification of memory handling compared with traditional server computer architectures and is scalable. And such simplification can result in energy saving argues Professor Goodacre.

Next: The Unimem model

The project has developed a universal memory model or Unimem to build on this by making a the memory a key focus of the architecture and dispensing with some traditional cache coherency requirements that have traditionally been implemented in servers.

In a presentation Professor Goodacre observed that there is no need for sequential consistency to be imposed in most data center workloads. Applications tend to partition datasets and it is best to place the processor and its cache near the dataset of a particular application task.

In other words, rather than moving data sets around at great energy expense in terms of moving data and imposing cache coherency requirements it is more energy efficient to keep the data set still and move the task to a processor that is near the required data set. "We have tried to come up with a software-centric architecture," said Professor Goodacre.

The Unimem approach not only maintains a consistent and coherent access from each compute node to its local DRAM but manages access to the system-wide memory resource. "Most importantly it can be implemented using available ARM technology with little additional hardware overhead," Professor Goodacre said.

Next: Would you like chiplets with that?

Chiplets

The project will make use of 64-bit ARM cores but makes the argument that at present levels of integration for servers chip costs are at the level $400 to $800 per unit and likely to double as production moves on to FinFET processes below the 20nm node. For reasons of yield the project sees a benefit in only implementing in leading-edge processes what needs to be and minimizing die size. These processor die become "chiplets" in the Euroserver nomenclature and sit on top of an interposer that carries peripheral circuitry.

In the physical implementation each chiplet will be an octa-core Cortex-A53 part implemented in 28nm FDSOI. And four of these chiplets will go on top of an interposer in a packaged part.

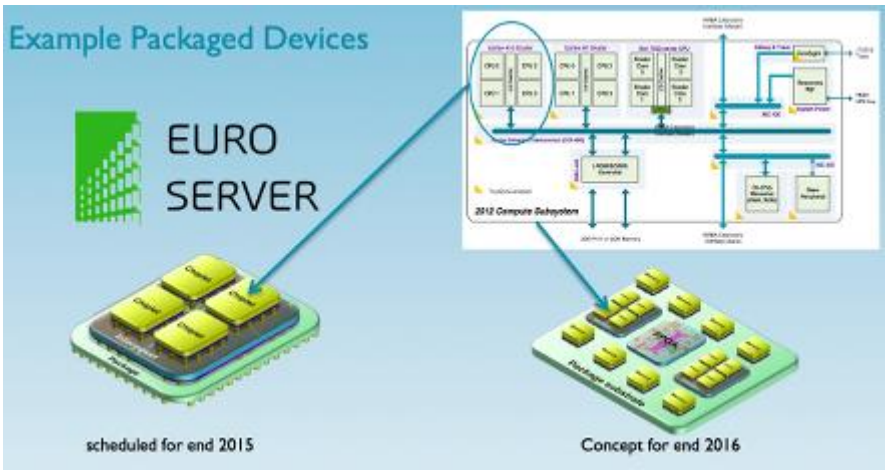


Figure 2: Server in a package, potentially including hybrid memory cubes

The Euroserver project started in September 2013 and for its first year has been working to flesh out and validate the computer architecture. One of the aspects of the architecture is to try and minimize use of long-distance interconnect and such bus standards as PCIe which were largely designed and optimized for performance rather than per-bit transferred energy consumption.

"We've spent time looking at software access patterns and the communication between the islands of coherence. We can see how to achieve 100 nanoseconds compared with typical traditional figures of 500 microseconds," said Professor Goodacre.

Professor Goodacre said that the use of the ARM processor or the FDSOI process were not the most critical things in achieving a highly efficient and scalable architecture compared with the main thrust; how data is handled. However, having a low power processor on an intrinsically low power process all helps.

Next: How much does it cost?

"Using ARM allows us to design a low-power system," said Professor Goodacre. "And 28nm FDSOI gives us a very interesting power management lever with back biasing and retention modes. So it’s the FDSOI, the chiplets, the 3D stacking, the software that all together make the difference," said Professor Goodacre.

While European Commission funded projects are not supposed to be used as a means of subsidizing commercial operations, if it should spark European-based commercial success in datacenters at the expense of Intel's x86 ecosystem few tears will be shed across Europe which has seen the strength and depth of its electronics base decline for many years.

The total cost of the project is €12,925,771 (about US$15.6 million) of which European tax payers are expected to provide €8,599,929 (about US$10.4 million).