European Commission

FVLLMONTI

Call: **H2020-FETPROACT-2020-01**

Grant Agreement no. **101016776**

Deliverable D2.1

Thermal impedance and trap extraction

Start date of the project: 1st February 2021

Duration: 60 months
Project Coordinator: Cristell MANEUX - University of Bordeaux
Contact: Cristell MANEUX - cristell.maneux@ims-bordeaux.fr

DOCUMENT CLASSIFICATION

Title	**Thermal impedance and trap extraction**
Deliverable	**D2.1**
Estimated Delivery	31/05/2023 (M29)
Date of Delivery Foreseen	25/05/2023
Actual Date of Delivery	25/05/2023
Authors	Chhandak Mukherjee - P1 – Ubx Yifan Wang - P1 - UBx Houssem Rezgui - P1 - UBx
Approver	Cristell Maneux – P1 – UBx
Work package	WP2
Dissemination	CO (Confidential)
Version	V1.2
Doc ID Code	D2.1_FVLLMONTI_P1-MUKHERJEE-230531
Keywords	VNWFET, junctionless (JL), vertical nanowire (VNW), temperature dependence, self-heating, pulsed I-V measurement, Low-frequency S-parameters, thermal impedance, On-wafer measurement, Multiphysics simulations.

DOCUMENT HISTORY

Version	Date	Modification
1.0	15/05/2023	First version
1.1	22/05/2023	Intermediate revision
1.2	25/05/2023	Final version

DOCUMENT ABSTRACT

This document describes novel methodologies for the extraction of the thermal and trap informtion of the FVLLMONTI technology: the elementary JunctionLess (JL) Vertical NanoWires Field-Effect Transistor (VNWFET). These devices are fabricated at LAAS-CNRS in WP1 (Fabrication of VNW technologies from devices to logic blocks) for the purpose of parameter extraction in WP2 and to provide necessary inputs for WP3 (TCAD and compact modelling).

The methodologies developed for the T2.1 of this WP detail the extraction of thermal impedance of the VNWFETs. Owing to the fact that VNWFETs do not exhibit a classical thermal behavior, in the scope of WP2, novel extraction methods were specifically developed for this technology. As this is the first time thermal impedance has been reported experimentally for vertical junctionless nanowires, different DC and AC methods were employed to validate the results. In addition, numerical multi-physics simulations of the VNWFETs were used to study the nanoscale thermal transport that provided a stronger validation of the extracted thermal parameters. Ultra-fast pulsed I-V measurements were used to study the trap dynamics and to extract the drift of important electrical parameters (e.g. threshold voltage). The extraction methodologies in this deliverable are particularly important for the FVLLMONTI value chain to ensure accurate compact modeling of the dynamic behavior of the JL-VNWFETs and associated logic circuit simulations.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101016776.

TABLE OF CONTENT

DOCUMENT CLASSIFICATION 2
DOCUMENT HISTORY 2
DOCUMENT ABSTRACT 2
TABLE OF CONTENT 4
LIST OF FIGURES AND TABLES 5
LIST OF ACRONYMS / GLOSSARY 6
Introduction 7
Extraction of Thermal Impedance 8
I. Experimental details 8
II. Thermal resistance extraction Methodologies 8
III. Thermal impedance extraction from Low-frequency S-parameter 11
IV. Extraction of thermal Parameters of JL-VNWFEts 12
V. Extraction of equivalent electro-Thermal Network 14
VI. Validation of Thermal Extraction Through Multiphysics Simulation for Nano-scale Thermal Transport 16
Investigation of Trap Dynamics using Pulse Measurements 20
I. Pulsed I-V measurements 20
II. Analysis of Trap dynamics and Electrothermal Effects 21
Toward modeling of electrothermal and trapping effects in JL-VNWFET 23
Conclusions 25
Bibliography 27

LIST OF FIGURES AND TABLES

Table 1: Description of deliverables in WP2 and their topics 7
Table 2: Thermal Resistance extracted using different Methods 13
Table 3: Extracted values of the elements of the Electro-thermal Network 15
Table 4: Thermal parameters of different materials used in the COMSOL material library 18
Table 5: Extract of the Schedule of relevant Milestones from DoA Annex 1 part A 25
Table 6: Extract of the KPI table from DoA Annex 1 part B 26

Figure 1: (a) Drain current as a function of drain-source voltage at fixed gate biases and under a wide range of measurement temperatures for a p-type JLNT with NW diameters of 22 nm with 25 NWs in parallel; (b) Drain current as a function of different measurement temperatures for the p-type JLNT geometries under study at V_{GS} = - 2.2 V and V_{DS} = - 2.2 V. 9
Figure 2: (a) I_D-V_{GS} characteristics of a JL-VNWFET at two different measurement temperatures T_A showing the intersecting points (I_{DQ}, V_{GSQ}) of two curves with different V_{DS}; (b) Threshold voltage shift of the JL-VNWFETs under test (with different diameters and nanowires in parallel) as a function of ambient measurement temperature. 10
Figure 3: Extraction of isothermal electrical contributions from (a) real and (b) imaginary parts of the Y_{22} parameter using polynomial fit. 11
Figure 4: (a) Extracted thermal resistances as a function of the effective transistor width, W_{eff} (= πDNF), as obtained from the four experimental DC methods and the LF S-parameter method in comparison with theoretical predictions and COMSOL simulations; (b) Rise of internal device temperature as a function of dissipated power 13
Figure 5: (a) Magnitude and (b) Phase of the extracted thermal impedance (Z_{TH}) of the JLNTs at V_{GS} =-2V and V_{DS} = -2V comparing measurement results and elctrothermal network simulations 14
Figure 6: Equivalent electrothermal R-C network of the vertical JLNT depicting contributions from the nanowires and PtSi contact regions. 14
Figure 7: Thermal (a) resistances and (b) capacitances of the electrothermal network as a function of the effective device width showing the two sets of contributions from the nanowire and PtSi regions, as extracted from LF S-parameters and COMSOL simulations in comparison with theoretical values. 15
Figure 8: (a) Comparison of effective thermal conductivity for silicon nanowire at room temperature; (b) Thermal conductivity as a function of diameter. 17
Figure 9: Extracted thermal resistance in SOI FinFETs [35] and JL-VNWFETs as function of (a) $NFin\ /NW$ and (b) $WFin/\ D$; (c) The extracted temperature in SOI FinFETs [35] and JLNTs as function of $NFin\ /NW$ for $Vds = -1.5\ V$ 19
Figure 10: (a) Effective thermal conductivity along the nanowire for different diameters; temperature distribution in single nanowire. (b) D= 17 nm. (c) D= 22 nm and (d) D= 34 nm. The arrows indicate the direction of the heat propagation. 19
Figure 11: (a) Pulsed measurements setup; (b) I_D-V_D under DC and pulsed conditions with pulse widths varying from 1µs to 10ms at V_G=-1V and -2.2V. 21
Figure 12: (a) Pulsed I_D-V_D measurements compared with compact model and COMSOL simulations; (b) Thermal conductivity and internal device temperature of the VNWFET. 21
Figure 13: (a) V_{TH}-t_{pulse} for different VNWFET geometries extracted from DC and pulsed measurements; (b) ΔV_{TH}-t_{pulse}, N_T-t_{pulse} for the device with a NW diameter of 22nm and 25 NWs in parallel compared with analytical solutions. 22
Figure 14: electrical equivalent circuit for the implementation of (a) self-heating and (b) trapping effects. 24
Figure 15: Evolution of drain current with (a) - (b) measurement temperatures and (c) different pulse widths, comparing experimental results, multiphysics and compact model simulations for a p-VNWFET with 25 parallel nanowires of 22 nm diameter 25

LIST OF ACRONYMS / GLOSSARY

ADS: Advance Design System
ANN: Artificial Neural Network
BTE: Boltzmann Transport Equation
D: Deliverable
DFT: Density functional theory
DTCO: Design-Technology Co-Optimisation
DUT: Device under Test
EDP: Energy-Delay Product
ETC: Effective Thermal Conductivity
FEM: Finite Element Method
FET: Field-Effect Transistor
GAA: Gate All-Around
GKE: Guyer and Krumhansl Equation
GPIB: General Purpose Interface Bus
GSG: Ground-signal-ground
JL: JunctionLess
L: Lead
M: Month of the project
MFP: Mean free path
P: Partner
PDE: the partial differential equation
PDP: Power-Delay Product
PMU: Pulse Monitor Unit
PU: Public
RF: Radio-Frequency
SBH: Schottky barrier height
SHE: Self-Heating Effects
SMU: Source Monitor Unit
SOLT: Short-Open-Load-Thru
SPICE: Simulation Program with Integrated Circuit Emphasis
TCAD: Technology Computer-Aided Design
V: Version
VN: Vertical Nanowire
VNA: Vector Network Analyzer
VNWFET: Vertical Nanowire Field Effect Transistor
WP: Work Package
ZTC: Zero-Temperature Coefficient

Introduction

WP2 aims to provide experimental data and extracted parameters from device fabricated in WP1 for the model validation in WP3, through extensive and specific characterizations on a wide range of device geometries operating under a wide range of bias conditions. Electrical reliability test will be performed to gather hardware data for the reliability-aware design tasks in WP3 and WP4. Additionally, WP2 will estimate ultimate device dimensions achievable through extrapolation at device level, leveraging the design flow developed in WP3 by taking into account the extracted values of device parasitics.

This report focuses on one of the two first characterization and parameter extraction methods of this WP, which is extraction of thermal impedance and trap information using novel DC and RF measurement techniques (see Table 1 below).

Table 1: Description of deliverables in WP2 and their topics

Label	Est. delivery date	Description	Partners	Type	DL
D2.1 D2.2	**M29** M40	**Thermal impedance and trap extraction**	**UBx, LAAS**	**R**	**PU**
D2.3 D2.4	M26 M44	Parasitic element extraction	UBx, LAAS	R	PU
D2.5	M56	Report on power-delay/energy-delay products at device-level	UBx, GTS, LAAS	R	PU
D2.6	M56	Report on extrapolated 3D logic cell performance to realistic dimensions	GTS, UBx, INL	R	CO
D2.7	M50	Report on VNWFET reliability tests and failure mechanisms	UBx, LAAS	R	PU

IMS laboratory at the University of Bordeaux has a strong experience in characterization, parameter extraction and modeling of nano-scale electronic devices. For the WP2, which is dedicated to parameter extraction of the gate-all-around (GAA) JL-VNWFET devices, different conventional as well as novel methods of characterization were explored. For this deliverable, particular focus was on the electro-thermal characterization of JL-VNWFETs, in order to accurately extract thermal and trap-related parameters leveraging on-wafer DC and S-parameter measurements under a wide range of temperature across all available device geometries.

In the era of emerging computing paradigms and artificial neural networks (ANN), gate-all-around (GAA) vertical nanowire field effect transistors (VNWFET) are envisioned as a future mainstream solution [1] to overcome Von Neumann bottlenecks for in-memory, energy efficient low-latency computing systems, owing to their naturally 3D architectures [2]. To successfully integrate associated device models within the design-technology-co-optimization (DTCO) flow and facilitate 3D logic circuit design using this technology, VNWFET compact models [3] need to capture a wide range of device physics, among which electrothermal effects [4] is a prerequisite due to its prominence in heavily scaled sub-20 nm device dimensions. Indeed, the electrical performances of aggressively scaled transistors are strongly impacted by self-heating, ultrafast thermal transport and thermal conductivity degradation, all of which link to electron-phonon coupling which is not well understood at the nanoscale. Additionally thermal confinement and electron-phonon coupling in sub-20 nm devices can further enhance trapping creating lattice distortion through what is known as the self-trapped electron phenomena [5]. Trap-assisted electro-thermal transport can therefore induce an additional drift in device electrical parameters such as threshold voltage. Recently, the operation of junctionless

transistors under low and high temperatures is getting particular attention [6-7], owing to their non-classical electro-thermal behavior and the absence of zero temperature coefficients (ZTC). In particular, ZTC points, at which drain current remains constant despite the change in temperature at fixed bias, are of particular interest for certain analog circuits such as operational transconductance amplifier [8]. The absence of ZTCs in JL transistors [9] have been attributed to a stronger temperature dependence of its threshold voltage and almost negligible variation in mobility with temperature [6-7]. As a result, conventional thermal extraction methods are not directly applicable for the JL-VNWFETs developed in the FVLLMONTI project and thus requires one to develop novel electro-thermal extraction methods.

In the scope of T2.1 of the FVLLMONTI project WP2, the following objectives are targeted:

- **To study the temperature and trapping induced drift of key device electrical parameters such as threshold voltage**
- **To extract thermal resistance and capacitances of the JL-VNWFETs leveraging various DC and AC methods in order to construct its equivalent electro-thermal network for compact model improvement and subsequent circuit simulations**

Extraction of Thermal Impedance

I. EXPERIMENTAL DETAILS

On-wafer Measurement Setup for DC and low-frequency S-parameters:

For both on-wafer DC and low-frequency S-parameter measurements, the Karl Suss PA-200 semi-automatic probe-station of the NANOCOM platform at the IMS laboratory was used. The DC setup included the semiconductor parameter analyzer HP4142 SMUs, controlled through a GPIB interface, for biasing the VNWFETs and recording the drain current characteristics while the chuck temperature was varied using a temperature controller in the 15-100 °C range.

The on-wafer low-frequency (LF) S-parameter measurement setup consists of the semiconductor parameter analyzer, HP 4142, for DC biasing and a vector network analyzer, Agilent E5061B (5Hz-3GHz). In order to couple RF and DC bias, bias tees (bandwidth of 30 kHz to 3 GHz) were used. The thermal impedance was extracted in the 30 kHz-300 MHz range beyond which pure electrical effects dominate the measured S-parameters. A standard SOLT calibration [10] was used with an RF input power of -28 dBm, followed by open-short de-embedding. DC bias points were chosen with high gate and drain biases where the effect of self-heating is most likely present. The measured S-parameters were then converted to Y-parameters that are used for studying the dynamic thermal response at low frequencies.

II. THERMAL RESISTANCE EXTRACTION METHODOLOGIES

Temperature-dependence of drain current:

In conventional CMOS technologies, with increasing temperature, the drain current reduces as a net result of the reduction of threshold voltage and a reduction of the mobility due to increased phonon scattering at higher temperatures [11]. In contrast, in junctionless transistors, it has been reported in [6] that a linear increase of drain current can be observed with temperature, similar to what has also been observed from our measurements (Fig. 1 (a)). This behavior is attributed to a strong temperature dependence of the threshold voltage [9] and an almost negligible variation in mobility with temperature [6-7]. In particular, weak temperature dependence has been attributed to the results of two competing mechanisms, phonon and impurity scattering, which have $T^{-3/2}$ and $T^{3/2}$ dependences, respectively, thereby compensating each other [12]. From DC measurements of all JL-VNWFET geometries, we observed a linear dependence of the drain current with measurement temperature (Fig. 1(b)).

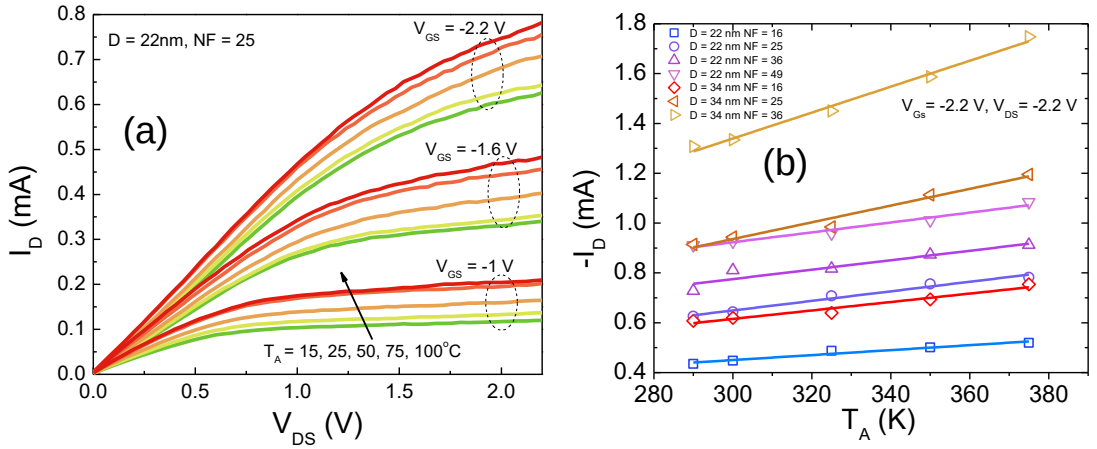

Figure 1: (a) Drain current as a function of drain-source voltage at fixed gate biases and under a wide range of measurement temperatures for a p-type JLNT with NW diameters of 22 nm with 25 NWs in parallel; (b) Drain current as a function of different measurement temperatures for the p-type JLNT geometries under study at V_{GS} = - 2.2 V and V_{DS} = - 2.2 V.

DC Method 1 (M1)

As a first estimation of the thermal resistance of the JL-VNWFETs, we calculated the ratio of the change in temperature to that of the dissipated power. For this, the variation of drain current with temperature was extracted at a fixed drain voltage from DC (I_D-V_D and I_D-V_G) measurements. Then the thermal resistance was estimated from the relation,

$$R_{TH} = \frac{\Delta T}{\Delta P_{diss}} = \frac{1}{V_D}\frac{\Delta T}{\Delta I_D} \quad (1)$$

Where, P_{diss} is the power dissipation which is calculated as a product of the drain current and the drain voltage. The second term in eq. (1) was then extracted from the slope of the current vs. temperature plot at a fixed high drain and gate bias. The results are in coherence with theoretical predictions [13] albeit overestimating theoretical values slightly for smaller geometries. This can be attributed to the fact that the variation in the drain current with the temperature is not free of uncertainties and fluctuations during the measurements, especially in smaller geometries featuring lower current levels. Despite a reasonable first estimation of thermal resistance using this method (M1), we explored other extraction methods for more precision.

DC Method 2 (M2)

With the second method (M2), we leverage I_D-V_G characteristics at different measurement temperatures (T_A) to estimate the thermal resistance from intersecting points between these curves (Fig. 2(a)) using the relation of junction temperature (T_j), i.e. the internal device temperature, given as

$$T_j = T_A + P_{diss}R_{TH}, \quad (2).$$

The principle of this method is based on the fact that at the intersecting points, the drain current and gate voltages (I_{DQ}, V_{GSQ}, respectively) are the same for two different sets of drain voltages (V_{DS1} and V_{DS2}) and measurement temperatures (T_{A1} and T_{A2}). As a first step, we theorize that the two junction temperatures (T_{j1} and T_{j2}) at the intersecting point are equal, with the increase in measurement temperature (T_A) compensated by the reduction in drain voltage for the two intersecting curves. For this compensation, we also consider that the R_{TH} should be extracted at a bias point with V_{GS} and V_{DS} as high as possible and that intersecting points at lower bias would give overestimated values. The thermal resistance can thus be extracted by equating the two junction temperatures at the intersecting point from $R_{TH} = (T_{A2} - T_{A1})/\, I_{DQ}(V_{DS1} - V_{DS2})$. However, to avoid making this assumption, we consider a third DC method (M3) in which we leverage another intermediate physical device parameter such as the threshold voltage, as stated in [6-7] that would reflect variations with both temperature and drain bias at constant gate bias.

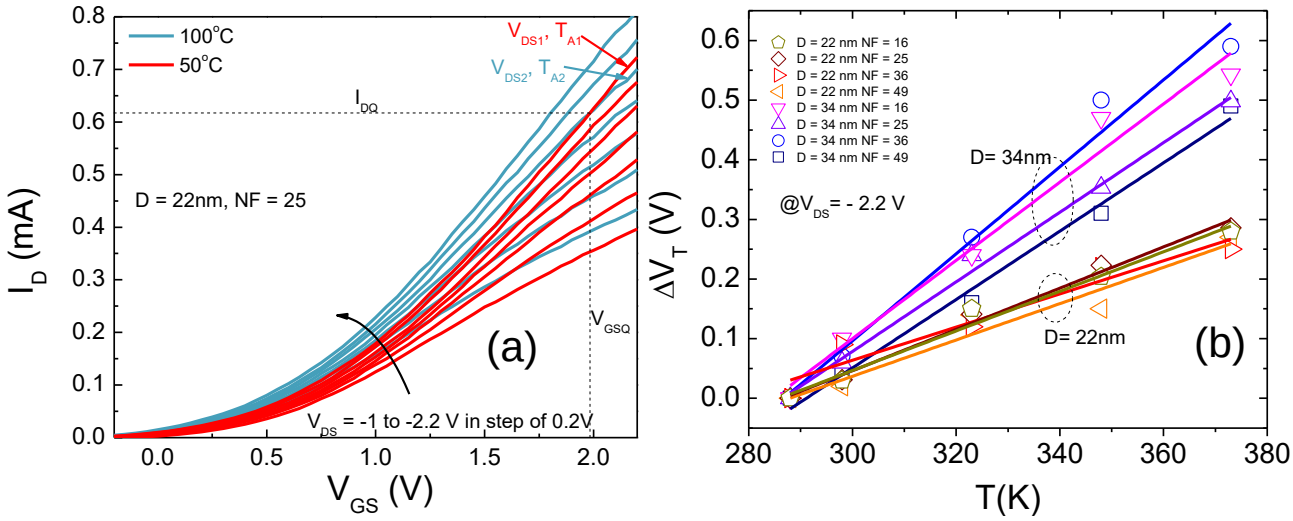

Figure 2: (a) I_D-V_{GS} characteristics of a JL-VNWFET at two different measurement temperatures T_A showing the intersecting points (I_{DQ}, V_{GSQ}) of two curves with different V_{DS}; (b) Threshold voltage shift of the JL-VNWFETs under test (with different diameters and nanowires in parallel) as a function of ambient measurement temperature.

DC Method 3 (M3)

Since the temperature dependence of drain current is principally governed by threshold voltage variation (ΔV_T) in the JLNTs, for method (M3), we extracted the temperature dependence of the threshold voltage from our measurements using the transconductance method [14]. This method relies on estimating the threshold voltage corresponding to the point where the value of the quantity (g_m/I_D) has reduced to half its peak value and is particularly suited to junctionless devices and is often preferred to other methods that produce more noisy data introducing additional uncertainty in threshold voltage extraction. Nonetheless, the transformed $g_m/I_D - V_{GS}$ plots also exhibited oscillation, especially for smaller devices and a hyperbolic smoothing function was used to extract an average value of the V_T [14]. The extracted threshold voltage values show a linear dependence with the temperature depicting a positive slope, similar to what has been reported for p-type JL transistors in [8]. Using the slope of these curves (Fig. 2(b)), the values of the thermal resistance can be estimated as,

$$R_{TH} = \frac{\Delta T}{\Delta P_{diss}} = \frac{1}{I_D}\frac{\Delta V_T}{\Delta V_D} \Big/ \frac{\Delta V_T}{\Delta T} \quad (3)$$

DC Method 4 (M4)

This method (M4) relies on estimating the slopes of the drain current as a function of the measurement temperature at a constant high drain and gate bias. The increase of the drain current shows a linear increase with the temperature for all devices (Fig. 1(b)). It is then possible to represent the total drain current as a linear function of the measurement temperature, T_A, as,

$$I_D = I_{D0}(1 + m_A(T_A - T_{A0})) \quad (4)$$

Where, I_{D0} is the drain current at a nominal temperature, T_{A0}, (in this case, at 15°C), and m_A is the slope of the I_D-T_A curve that can be calculated as $m_A = \frac{dI_D}{dT_A} / I_{D0}$. In the same temperature range, the junction temperature is governed by (2) in which P_{diss} (V_{DS}×I_D) is also a linear function of T_A at fixed V_{DS} and one can assume that I_D is a linear function of the junction temperature as well. So a linear relation between these two exists as,

$$I_D = I_{D0}\big(1 + m_j(T_j - T_{j0})\big) \quad (5)$$

Where m_j is the slope of the I_D-T_j curve. Now, using (2), the change in the device temperature can be written as,

$$T_j - T_{j0} = T_A - T_{A0} + V_{DS}R_{TH}(I_D - I_{D0}), \quad (6)$$

Substituting (6) in (5) gives,

$$I_D = I_{D0}(1 + m_j(T_A + T_{A0} + V_{DS}R_{TH}(I_D - I_{D0}))), \quad (7)$$

Differentiating with respect to T_A, we obtain,

$$\frac{dI_D}{dT_A} = I_{D0} m_j (1 + V_{DS} R_{TH} \frac{dI_D}{dT_A}) \equiv \frac{dI_D}{dT_A} = \frac{I_{D0} m_j}{1 - I_{D0} m_j V_{DS} R_{TH}} \quad (8)$$

Replacing $\frac{dI_D}{dT_A} / I_{D0}$ by m_A, one can write,

$$\frac{1}{m_A} = \frac{1}{m_j} - I_{D0} V_{DS} R_{TH} . \quad (9)$$

In (9), m_A can be extracted from the measured I_D-T plots at different V_{DS} values and from the slope of $1/m_A$ vs. $I_{D0}V_{DS}$, one can extract the R_{TH}.

III. THERMAL IMPEDANCE EXTRACTION FROM LOW-FREQUENCY S-PARAMETER

Low-frequency (LF) S-parameter measurements are an effective way of studying dynamic self-heating in modern transistors [15]. LF S-parameter measurement method has been proven to be quite effective for isolating pure electrical and non-linear electrothermal effects and eventually estimate the values of the elements of the thermal networks in bipolar [16] and MOS transistors [15]. Thermal impedance is a particularly crucial parameter for device compact models when evaluating circuit performances under dynamic conditions. In a two-terminal device, at higher frequencies, where thermal response is too slow compared to the operating frequency, the frequency response is dominated by the device capacitance. Hence, S-parameters measured at lower frequencies are used to capture the dynamic self-heating. Pure electrical characteristics of the device dominate at higher frequencies in the Y-parameter vs. frequency plot. So the frequency that separates these two mechanisms, i.e. an isothermal frequency (f_{iso}), can be identified from the $Y_{22}(f)$, i.e. drain conductance, as illustrated in Fig. 3. Essentially, in the low frequency range before f_{iso}, one can extract parameters of dynamic thermal response, while above f_{iso}, pure electrical, i.e. isothermal, characteristics of the device dominates.

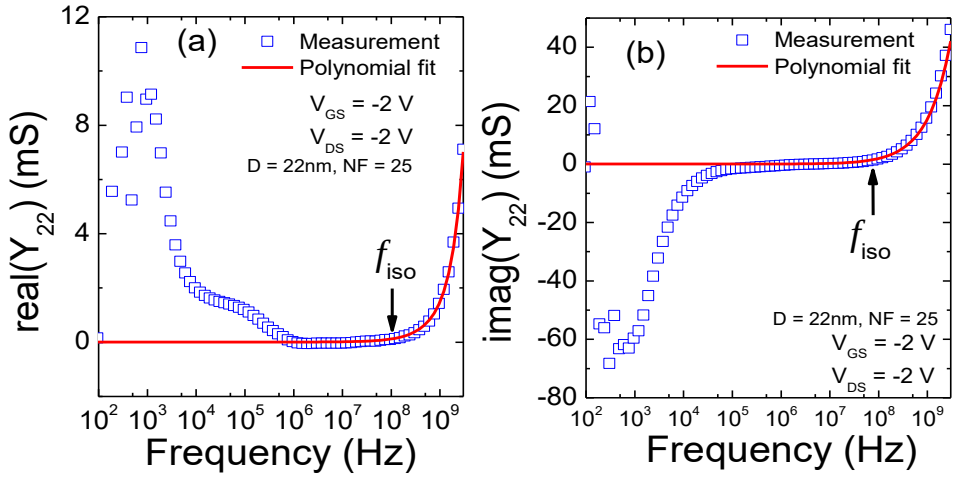

Figure 3: Extraction of isothermal electrical contributions from (a) real and (b) imaginary parts of the Y_{22} parameter using polynomial fit.

Essentially, in the low frequency range before f_{iso}, one can extract parameters of dynamic thermal response, while above f_{iso}, pure electrical, i.e. isothermal, characteristics of the device dominates. On the basis of the theoretical analysis in [17], the thermal impedance of a FET can be represented in terms of its Y parameters as,

$$Z_{TH}(f) = \frac{\left[Y_{22}(f) - Y_{22}^{iso}(f)\right]}{\frac{dI_D}{dT_A}\left[I_{DS} + V_{DS} Y_{22}(f) + V_{GS} Y_{12}(f)\right]} \quad (10)$$

The $Y_{22}^{iso}(f)$ is the isothermal electrical part that can be estimated by fitting polynomials to the real and imaginary parts of Y_{22} (Fig. 3) and then reconstructing $Y_{22}^{iso}(f)$ [15]. The dI_D/dT_A term has been extracted from the DC measurements as illustrated in Fig. 1(b). Finally, from (10), the thermal impedance can be calculated from LF S-parameters.

IV. EXTRACTION OF THERMAL PARAMETERS OF JL-VNWFETS

R_{TH} Extraction

DC measurements on the JLNTs at different measurement temperatures revealed a steady increase of the drain current with temperature. Contrary to classical MOSFET operation, where mobility degradation at higher temperature due to increased impurity scattering results in a reduction of the drain current, in the junctionless transistors, lattice and impurity scattering compensate each other resulting in an almost negligible change in the mobility. On the other hand, a linear shift of threshold voltage with increasing temperature contributes to the increasing drain current. So, from drain current variation with temperature at high gate and drain bias, the first method (M1) described in section II was used to estimate the thermal resistance of these JL VNWFETs. These were then compared to theoretical values of the thermal resistance calculated using [13]

$$R_{TH_{theo}} = \frac{L}{\kappa_{Si}\pi R^2 NF} + \frac{1}{4\kappa_{PtSi}R\cdot NF} \quad (11)$$

Here, L is the nanowire length, R is the nanowire diameter, NF is the number of nanowires in parallel, and κ_{Si} is the thermal conductivity of bulk silicon with a value of 130 $Wm^{-1}K^{-1}$ [18] whereas κ_{PtSi} is the thermal conductivity of PtSi contact region with a value of 30 $Wm^{-1}K^{-1}$ [18]. The first part of the equation signifies the contribution of the nanowires whereas the second contribution is due to the PtSi contact region. The extracted values of the thermal resistance using the first DC method (M1) are compared with the theoretical calculations for the JLNT geometries characterized in Fig. 4(a), which shows the extracted values slightly overestimating results especially for smaller geometries where uncertainty in drain current values due to a loss of measurement reproducibility becomes predominant, thus leading to possible underestimation of the slope of the I_D-T plot.

Next, we followed the second DC method (M2). This method provided higher precision when compared with theoretical values for both sets of devices with nanowire diameters of 22 and 34 nm (Fig. 4(a)). Again, higher uncertainty was observed for smaller geometries but the results are closer to the theoretical predictions compared to the first method (M1). Without the assumption that the internal device temperature be equal for the two sets of intersecting curves the third method (M3) provided more reliable results. The results obtained using M3 provides similar overall accuracy as M2 while showing higher precision for smaller geometries. This is likely because of the relative errors of the terms $\frac{\Delta V_T}{\Delta V_D}$ and $\frac{\Delta V_T}{\Delta T}$ balancing each other.

The fourth DC method (M4) described by eqs. (4) - (9) was employed for extracting thermal resistances of the JLNTs. This method provides results of better accuracy compared to the first method but slightly higher values than the theoretical or the M3 for smaller geometries (Fig. 4(a)), probably because it also involves estimating the slope of the I_D-T curve and incorporates the uncertainty in the measurements of I_{D0} that are crucial for accurate extraction.

Lastly, the internal device temperature rise, calculated using (2), is shown in Fig. 4(b) for all geometries as a function of dissipated power, indicating a significant temperature increase at high bias conditions (confirmed through multiphysics simulations in [19]) leading to possible device self-heating.

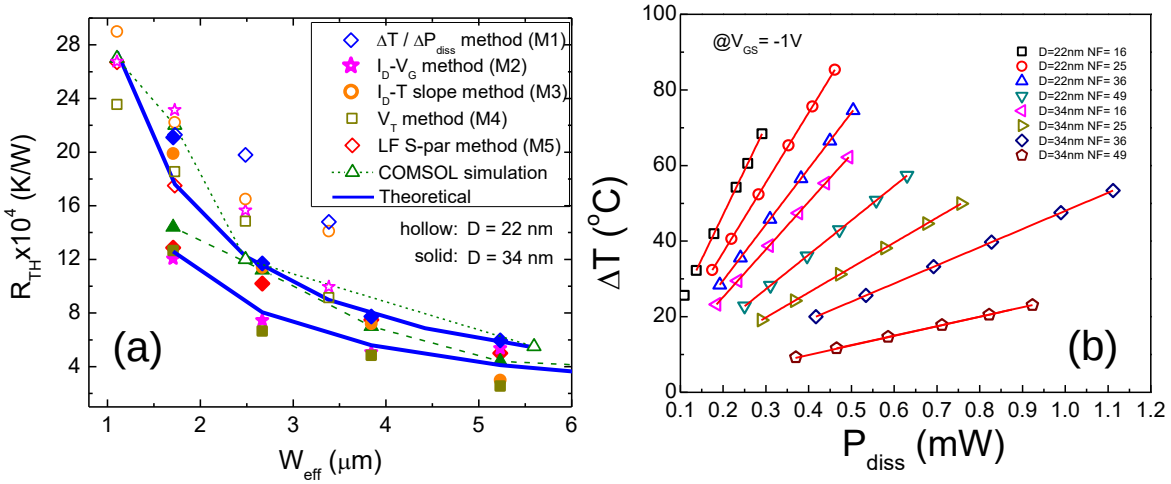

Figure 4: (a) Extracted thermal resistances as a function of the effective transistor width, W_{eff} (= πDNF), as obtained from the four experimental DC methods and the LF S-parameter method in comparison with theoretical predictions and COMSOL simulations; (b) Rise of internal device temperature as a function of dissipated power.

Table 2: Thermal Resistance extracted using different Methods

Geometry		DC methods (K/W ×10⁴)				Theoretical (K/W ×10⁴)	AC (LFS) method (K/W ×10⁴)	COMSOL
D (nm)	NF	M1	M2	M3	M4			
22	16	21.3	23.1	22.2	18.5	27.5	17.5	22
22	25	19.8	15.6	16.5	14.8	17.6	-	12
34	16	11.7	7.4	11.4	6.6	12.6	10.2	11.2
34	25	7.75	5.1	7.2	4.8	8.06	7.5	7

Z_{TH} Extraction

The LF S-parameter measurements described in section III were leveraged to extract the thermal impedance of the JL-VNWFETs using (10). Keeping in mind that the accuracy of this method also depends on the accurate estimation of the slope dI_D/dT_A extracted from DC measurements as well as removing the pure electrical contribution of the output conductance (Y_{22}^{iso}) from the S-parameter measurements, magnitude and phase of the thermal impedance were extracted as shown in Figs. 5 (a) and (b). The R_{TH} can be extracted from the magnitude of the Z_{TH} at low frequencies (0.1-10 kHz range) where dynamic self-heating is less predominant and static thermal response dominates. Hence, from the constant value of the magnitude of Z_{TH} in the 100-1000 Hz frequency range (Fig. 5(a)), one can estimate the R_{TH} for each NW dimension. The extracted values are compared with the other extracted values of the R_{TH} from the previously described DC methods in Fig. 4(a) and Table 2, highlighting that the values estimated using LF S-parameter method are in the same range as the first DC method.

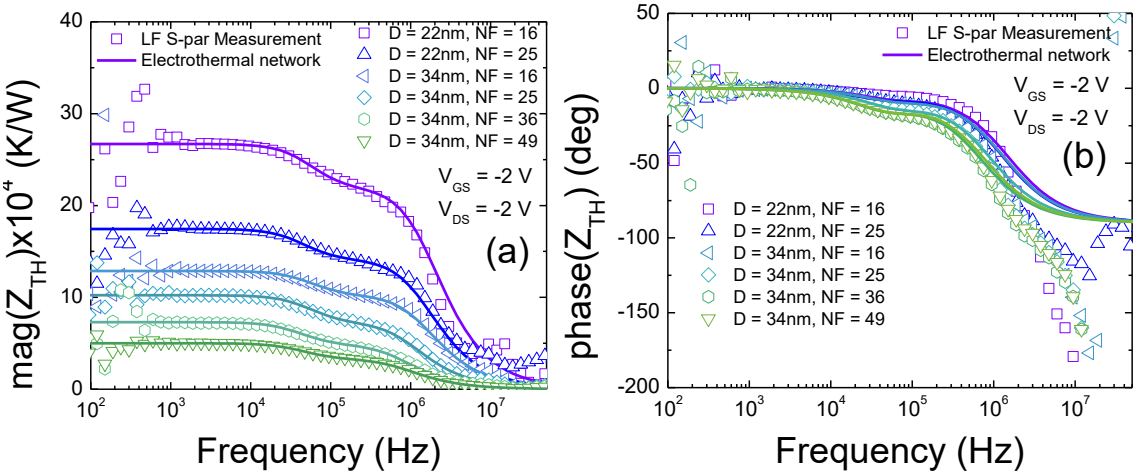

Figure 5: (a) Magnitude and (b) Phase of the extracted thermal impedance (Z_{TH}) of the JLNTs at V_{GS} =-2V and V_{DS} = -2V comparing measurement results and elctrothermal network simulations

V. EXTRACTION OF EQUIVALENT ELECTRO-THERMAL NETWORK

What is further interesting is that from the extracted thermal impedance one can also estimate the elements of the entire thermal network of the vertical device that constitutes its heat-flow dynamics. To do so, one can represent the Z_{TH} of the device by an equivalent electro-thermal network consisting of resistive (R_{TH}) and capacitive (C_{TH}) elements using a modified Foster-like equivalent electro-thermal network [20] of the JLNTs. The equivalent thermal network is a representation of the device self-heating which is commonly used to recalculate the internal device temperature (T_J) implemented through a fictitious node. For compact model implementation, thermal effects are emulated through electrical parameters of the equivalent circuit. Drawing an analogy with voltage and currents, in the thermal network, the dissipated power is represented as the equivalent of the node current whereas the node voltage of the network gives the device temperature calculated through the thermal resistance and capacitance. However, this implementation only considers a single pole for the frequency response of the thermal network, which is often not sufficient in modern transistors due to distributed nature of the thermal elements. For example, in our measured LF S-parameters, we observed that the frequency-dependent behavior of the Z_{TH} can only be captured with sufficient accuracy considering an equivalent two-pole electro-thermal network consisting of two resistive and two capacitive elements (Fig. 6).

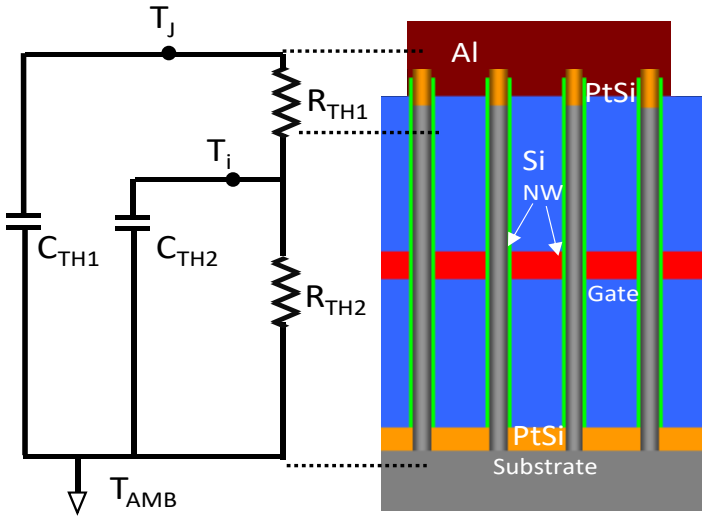

Figure 6: Equivalent electrothermal R-C network of the vertical JLNT depicting contributions from the nanowires and PtSi contact regions.

Using the two-pole thermal network shown in Fig. 6, we can calculate the total device thermal impedance Z_{TH} as

$$Z_{TH} = (Z_{TH2} + R_{TH1})/(1 + j\omega C_{TH1}(Z_{TH1} + R_{TH1})) \quad (12)$$

With, $Z_{TH2} = R_{TH2}/(1 + j\omega C_{TH2} R_{TH2})$.

Next, we simulated the magnitude and phase of the Z_{TH} using (12) and compared the results with the measurements shown in Fig. 5. Through model fitting we could then extract the parameters, R_{TH1}, R_{TH2}, C_{TH1} and C_{TH2}, of the equivalent thermal network which are shown in Table 3 and Fig. 7. To interpret the physical origin of these two sets of thermal resistances, we refer to the theoretical expression of (11) in which the first term refers to the thermal resistance of the nanowire whereas the second term comes from the contribution of the PtSi contact region. Comparing these two theoretical contributions separately (table 3 and Fig. 7 (a)) with the extracted values of R_{TH1} and R_{TH2}, we could clearly see a strong correlation for all geometries, thus validating the proposed electrothermal network, indicating that the two poles of the thermal impedance originates out of these two separate regions of the vertical junctionless nanowires. This is illustrated schematically in Fig. 6 with the Foster-like equivalent thermal network superimposed against different regions of the vertical device structure. To the best of our knowledge, this is the first report on the extraction of electro-thermal equivalent network in junctionless transistors. In the next section, numerical Multiphysics simulation results further corroborate these results.

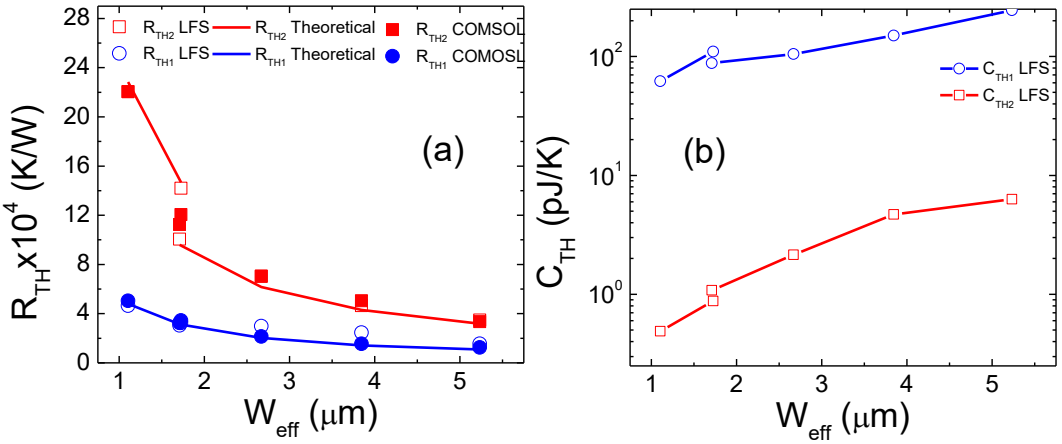

Figure 7: Thermal (a) resistances and (b) capacitances of the electrothermal network as a function of the effective device width showing the two sets of contributions from the nanowire and PtSi regions, as extracted from LF S-parameters and COMSOL simulations in comparison with theoretical values.

Table 3: Extracted values of the elements of the Electro-thermal Network

Geometry		LFS method (K/W ×10⁴)		Theoretical (K/W ×10⁴)		COMSOL		LFS method (pJ/K)	
D (nm)	NF	R_{TH1}	R_{TH2}	R_{TH1}	R_{TH2}	R_{TH1}	R_{TH2}	C_{TH1}	C_{TH2}
22	16	4.65	22.1	4.73	22.8	5	22	62	0.49
22	25	3.25	14.2	3.03	14.6	3.4	12	110	0.88
34	16	3.05	10.1	3.06	9.53	3.2	11.2	88	1.08
34	25	2.99	7.02	1.96	6.1	2.1	7	105	2.15
34	36	2.45	4.65	1.36	4.24	1.4	4.5	150	4.7

VI. VALIDATION OF THERMAL EXTRACTION THROUGH MULTIPHYSICS SIMULATION FOR NANO-SCALE THERMAL TRANSPORT

Theory and Computational Model

To understand the electrothermal behavior in JL-VNWFETs, we performed numerical multiphysics simulations of the device structure using finite element method (FEM) based COMSOL simulation considering the same conditions as the measurements. The simulations are carried out using the partial differential equation (PDE) package in COMSOL governing the carrier transport equations by coupling thermal and electrical characteristics and solving the non-Fourier heat equation and the drift-diffusion model with interface trapping effects [21]. For this, we used a novel hydrodynamic equation of the Guyer and Krumhansl (GKE) to predict non-Fourier heat dissipation which solves the linearized Boltzmann transport equation (BTE) for non-equilibrium heat transport [22]. Many of the past works have focused on phonon hydrodynamics when both normal and resistive scattering processes have strong contributions to the physical origin of the heat response [23]. In recent studies, the GKE was developed based on macroscopic hydrodynamic equation for nanoscale heat transport at room temperature [24, 25] where most nanoelectronic devices commonly operate. The governing equations are the GKE and the energy-conservation equation, respectively [24, 26-27] written as,

$$q + \tau_R \frac{\partial q}{\partial t} = -\kappa \nabla T + l^2 (2 \nabla \nabla . q + \Delta q) \quad (13)$$

$$c \frac{dT}{dt} + \nabla . q = 0 \quad (14)$$

where q is the heat flux, τ_R is the phonon relaxation time, κ is the thermal conductivity, ℓ is the phonon MFP, c is the heat capacity and T is the temperature. Equation (13) gives a simple analytical solution of the phonon BTE as well as a better understanding of non-Fourier heat-flow modeling. As device size decreases, non-local effects included in the Laplacian term Δq, become dominant. In general, the nonlocality of the heat flux gradient originates from the phonon-boundary scattering and confinement effects. Based on the average phonon MFP, ℓ , heat transport takes place in three regimes: (i) ballistic (external boundary scattering); (ii) quasi-ballistic and (iii) bulk-like (diffusive). In sub-20 nm silicon devices, ballistic transport governs heat flow, and it is expected that phonon-boundary scattering contributes to the reduction of the thermal conductivity [28]. For steady-state phonon transport, the GKE is expressed as

$$q = -\kappa \nabla T + l^2 \Delta q \quad (15)$$

The present GKE provides an enhanced formulation for investigating nanoscale heat transport beyond the classical Fourier's law.

Boundary Conditions

At room temperature, slip boundary conditions is mandatory for the description of phonon transport in small dimensional materials [24]. Particularly, two macroscopic mechanisms occur during non-equilibrium phonon distribution: (i) the tangential heat flux close to the boundary and (ii) the non-continuous temperature variation (i.e. temperature jump) due to phonon-boundary collision [24]. Based on the Maxwell model, the slip boundary condition for the tangential heat flux at the boundary is given by [29]

$$q_t = -C_w \ell \nabla q_t . n \quad (16)$$

$$q . n = 0 \quad (17)$$

where, n is the interface normal vector and C_w is a constant which is expressed in terms of the specularity of the surface. In most cases, solving the GKE and slip boundary conditions requires an accurate value of the thermal conductivity, average mean free path and heat capacity that are obtained from microscopic approaches such as *ab initio* calculations. In the computational model, the GKE is solved based on the finite-element method (FEM) using *COMSOL MULTIPHYSICS* simulator [30]. For the steady state phonon transport, we consider that the nanowires are initially at a constant temperature, T_c , and then one end of the nanowire comes in contact with the heat-source $T_h = T_c + \Delta T$ where ΔT is the temperature difference between the two ends of the nanowire.

Effective Thermal Conductivity Model

In the nanoscale JL-VNWFETs, where the characteristic lengths are comparable to the MPF, ballistic phonon transport can lead to a critical dependence of effective thermal conductivity on size effects [28]. For the heat flow through a nanowire with radius r, Eq. (15) can be rewritten as

$$q_x(r) = -\kappa \frac{dT}{dx} + l^2 \frac{d^2 q_x(r)}{dr^2} + l^2 \frac{1}{r} \frac{dq_x(r)}{dr} \quad (18)$$

The effective thermal conductivity (ETC), κ_{eff}, is defined as [29]

$$\kappa_{eff} = \frac{\int q_x(r) d\Gamma}{\frac{S\Delta T}{L}} \quad (19)$$

Here Γ is the cross section, S is the surface area and L is distance between the two ends of the system. The classical Fourier's law of heat conduction can only predict thermal conductivity in bulk materials when the characteristic dimensions are larger than the phonon MFP. Here, we consider a Knudsen number defined as $Kn = \frac{\ell}{D}$, where D is the diameter of the nanowire, to classify the nanoscale thermal transport within the nanowire [24]. For $Kn > 1$, ballistic transport dominates and the thermal conductivity is significantly influenced by the confinement effects. For $Kn \approx 1$, the thermal conductivity increases due to enhanced boundary scattering (i.e. weak confinement effect). In diffusive regime ($Kn \ll 1$), Eq. (18) reduces to the Fourier's law, $q_x(r) = -\kappa \frac{dT}{dx}$, where $\kappa = \kappa_{eff}$ (bulk thermal conductivity). According to Kwon *et al.*, [28], we assume fully diffusive boundary scattering, i.e., $C_w = 1$, to achieve an accurate comparison with the theoretical and experimental results (Fig. 8 (a)). Our proposed model displays a good prediction of experimental data for Si NWs down to 30 nm. From Fig. 8(a), we can distinguish between three distinct thermal transport regimes: (i) a ballistic regime where the phonon boundary/interface scattering leads to a significant reduction of the thermal conductivity; (ii) a quasi-ballistic regime where we expect a Lévy flight due to trapped phonons in the Si NW; (iii) a diffusive regime indicated by the effective thermal conductivity reaching its bulk Si value as the system size increases, where the Knudsen number is small enough ($K_n = 0.05$). The GKE gives a consistent result with the theoretical predictions and experimental data. For further comparison, the GKE is compared to experimental results [31] and the Callaway–Holland model [32]. Fig. 8 (b) shows the diameter dependence of normalized thermal conductivity in Si NWs with a phonon MFP, $\ell = 300\ nm$, at $T = 300\ K$. Clearly, the present model agrees well with the theoretical model and experimental data reported by Maire et *al.* [33]. The thermal conductivity decreases in small diameters due to phonon confinement. As system dimension reaches the sub-20nm regime, the effect of phonon/interface scattering in certain hotspots leads to reduced thermal conductivity which can then lead to pronounced self-heating.

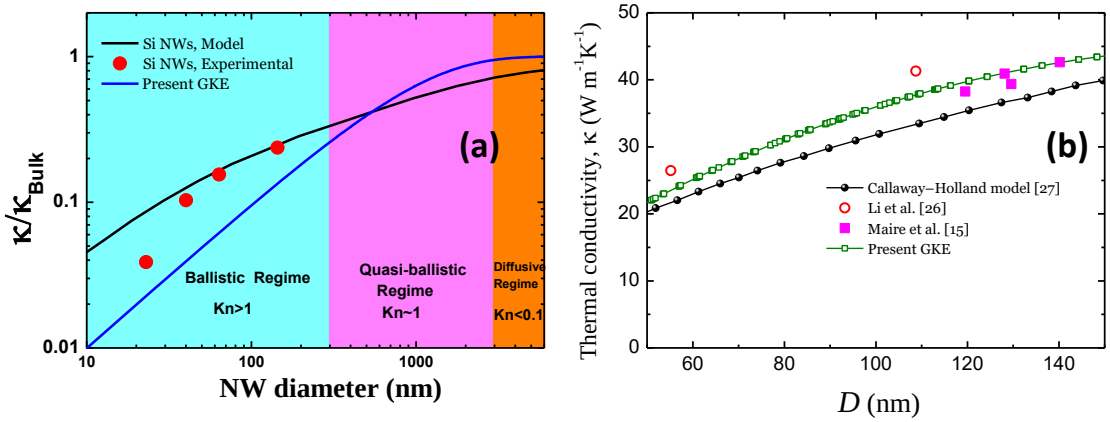

Figure 8: (a) Comparison of effective thermal conductivity for silicon nanowire at room temperature; (b) Thermal conductivity as a function of diameter.

Extraction of Thermal Resistance

For the device under test, the gate material is fabricated with chromium (Cr) that ensures better control of interfacial thermal transport within the nanowire and offers high thermal conductivity even at room temperature [29]. Moreover, the aluminum (Al) top, bottom and gate contacts is highly beneficial for

ensuring weak thermal degradation at higher temperatures. Consequently, for the Multiphysics simulations, the thermal properties of Al are obtained based on density functional theory (DFT) calculations with respect to BTE [34]. The thermal properties of the materials chosen for our simulation are listed in Table 4. The heat capacity values of silicide and Al are obtained from the material library in COMSOL. To solve the thermal transport equations for the JL-VNWFET device configuration, the heat transport is coupled with the electrical characteristics, rewriting eq. (14) as

$$C\frac{\partial T}{\partial t} + \nabla q = P \tag{20}$$

where P is the dissipated power defined as $P = V_{ds}\, I_{ds}$. To extract the thermal resistance of the device, the heat flux can be obtained as

$$q = \kappa_{eff}\frac{S\Delta T}{L} \tag{21}$$

The heat flux distribution is then given by

$$q = \frac{S\Delta T}{R_{th}} \tag{22}$$

where R_{th} is the thermal resistance in unit of (K/W).

Table 4: Thermal parameters of different materials used in the COMSOL material library

Symbol	κ ($Wm^{-1}K^{-1}$)	C ($J\,m^{-3}K^{-1}$)	ℓ (nm)
Si	150	1.692×10^{6}	185
SiO_2	1.4	1.75×10^{6}	0.4
PtSi	18.5	2.1×10^{6}	-
Cr	111	2.47×10^{6}	-
Al	252	2.43×10^{6}	10

As a first validation of the multiphysics simulation framework, we compare the extracted thermal resistance with that of the well-known SOI FinFETs. In order to ensure a reasonable comparison between both technologies, we consider a gate length of 90 nm and a $V_{ds} = -1.5\,V$. It is important to note that our developed model is solved under non-isothermal conditions. The interfacial thermal transport is governed by non-slip boundary condition given by Eq. (18). Here, the thermal resistance is extracted from the drain region where the temperature hot-spots are observed. Fig. 9 (a) compares the extracted thermal resistance as a function of the number of fins (for FinFETs) and nanowires (for JL-VNWFETs). The thermal simulations were performed using an extremely finer mesh with 65000 spatial grids around the transistor active area to facilitate solving the GKE model. The maximum lattice temperate is obtained from the dissipated power calculated from I_{ds}–V_{ds} characteristics. The thermal resistance reduces with increasing number of fins and nanowires with the maximum thermal resistance $R_{th,max}$, corresponding to fewer parallel nanowires and fins. When the number of nanowires increases, the phonon-boundary scattering becomes weak leading to enhanced reduced thermal resistance. In addition, the thermal degradation increases as the diameter reduces due to ballistic phonon transport dominating in sub 20 nm dimensions as observed from Fig. 9 (b). In particular, for small diameters, the thermal resistance increases due to phonon confinement effects occurring as a result of the surface roughness which, in turn, results in a loss of momentum and eventually a strong resistive transport at room temperature. Interestingly, the thermal resistance observed in both p-type SOI FinFETs and JLNTs is smaller than the R_{th} extracted for n-type SOI FinFETs. This is because of the fact that p-type devices have a higher thermal conductivity compared to n-type devices. Fig. 9 (c) plots the internal device temperature in FinFETs and JLNTs with respect to fins and nanowire numbers. The temperature increases with increasing N_{Fin} and NWs as the dissipated power P also increases. For $N_{Fin}/NWs = 2$ and 6, one can observe a temperature difference of around $8\,K$ between FinFETs and JL-VNWFETs, which reaches $17\,K$ for large number of fins and nanowires ($N_{Fin}/NWs = 20$ and 30). This shows that SOI FinFETs exhibit a higher temperature increase than that of JL-VNWFETs indicating better thermal stability for the latter case.

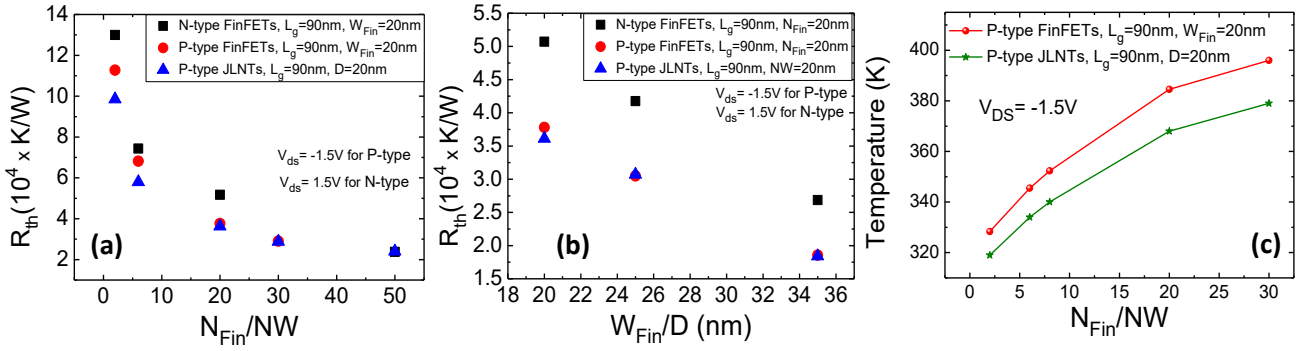

Figure 9: Extracted thermal resistance in SOI FinFETs [35] and JL-VNWFETs as function of (a) $N_{Fin}\ /NW$ and (b) $W_{Fin}/\ D$; (c) The extracted temperature in SOI FinFETs [35] and JLNTs as function of $N_{Fin}\ /NW$ for V_{ds} = $-1.5\ V$

Fig. 10 (a) shows the thermal conductivity of the JL-VNWFETs along the channel direction with 25 nanowires in parallel extracted from the device simulation. As expected, the lower effective thermal conductivity of the nanowire is directly liked to higher thermal resistance in small dimeters, which, in turn, may lead to pronounced SHEs. It is to be noted that, the effective thermal conductivity reaches 3.26 W/m/K and 11.6 W/m/K for $D = 17\ nm$ and $D = 34\ nm$, respectively. The reduction of the thermal conductivity is mostly caused by phonon confinement effects in the drain area (the hot-spot region). Close to the drain area, phonons are transported in a ballistic way and boundary scattering takes place which influences the thermal conductivity. The phonon-boundary scattering rate is significantly high in small dimensional materials which can be held responsible for the weak value of the ETC for $D = 17\ nm$. For subsequent analyses on the heat propagation, we focused on a single nanowire. Figs. 10 (b)-(d) plot the simulated distribution of internal device temperature in JL-VNWFETs for different diameters. The maximum temperature is detected near the drain region which then gradually diminishes toward to the channel layer. Interestingly, the effective temperature rise with increasing diameter is the combined effect of increasing dissipated power P and reducing thermal resistance in larger diameters. For smaller diameters, in Fig. 10 (b) and Fig. 10 (c), the heat flow is localized in the drain side which then propagates along the nanowire. However, in Fig. 10 (d) for largest diameter (34 nm), the heat accumulation spreads over the drain side only. Furthermore, temperature distributions for smaller diameters are indicative of the thermal confinement near the drain region that leads to elevated temperature higher thermal energy. Further reduction in internal device temperature can be achieved by increasing the diameter and number of nanowires in parallel.

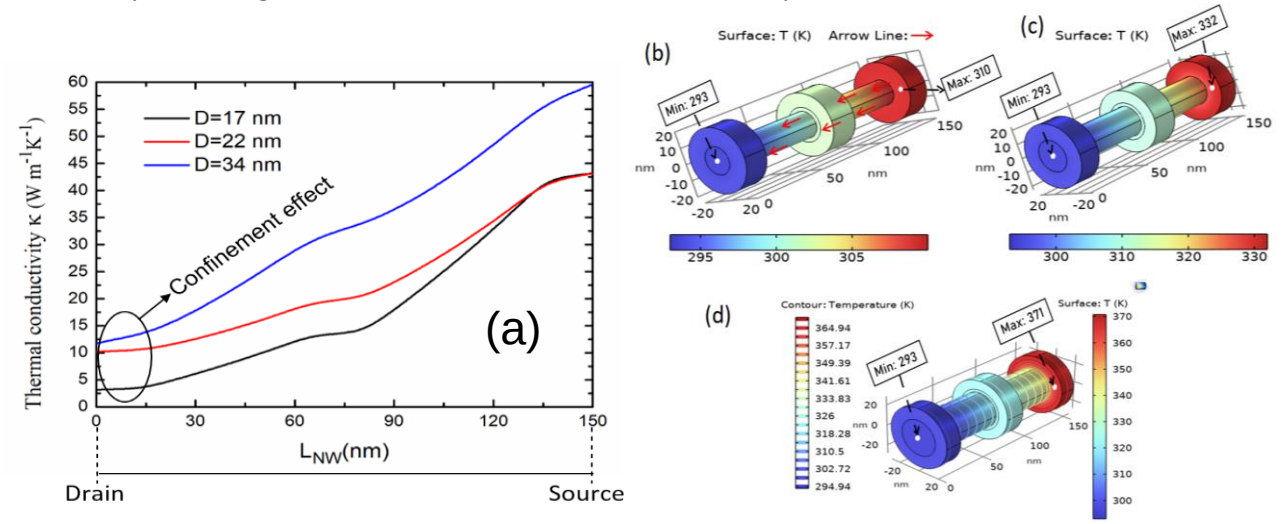

Figure 10: (a) Effective thermal conductivity along the nanowire for different diameters; temperature distribution in single nanowire. (b) D= 17 nm. (c) D= 22 nm and (d) D= 34 nm. The arrows indicate the direction of the heat propagation.

Finally, the thermal resistance values extracted using COMOSOL are compared in Fig. 4 (a) and Fig. 7(a) with experimentally extracted values (table 2 and 3), showing very good agreement, thus validating the novel experimental methods proposed in this deliverable for thermal parameter extraction in JL-VNWFETs.

Investigation of Trap Dynamics using Pulse Measurements

In addition to electrothermal effects, we studied trapping-induced drift of device electrical parameters through pulsed I-V measurements in order to dissociate trapping and thermal effects by applying short gate pulses to the devices. It is to be noted that at steady state the Si/SiO_2 interface trap density has already been extracted for the JL-VNWFETs from LAAS. The principle motivation for using pulse measurements as a complementary tool for extracting trap information is to accurately characterize trap activation under dynamic conditions, which is crucial for logic circuit simulations using the transistor compact model developed in the scope of the task T3.2 of FVLLMONTI.

I. PULSED I-V MEASUREMENTS

The principle of pulsed I-V measurements relies on applying very short gate pulses on the device so as not to allow sufficient time for its internal temperature to change significantly or activate any charge trapping. Fig. 11 (a) shows the experimental pulse measurement setup using the Keithley 4200A-SCS parameter analyzer. A short square-wave pulse voltage with varying amplitude in the -1V to 2.2V range and a pulse width varying between 1µs and 10ms with a duty cycle of 10%, is applied at the gate. A staircase pulse stepping voltage was applied at the drain terminal to minimize the charging effect [36]. The I_D-V_D measurement data for all available geometries (nanowire diameters of 22 and 34 nm with 16 and 25 NWs in parallel) over the entire bias range showed a constant increase in the drain current with pulse width and gradually approaching the characteristics obtained under DC conditions. In conventional transistors, however, the reduction in mobility with increasing pulse width leads to a decrease in drain current. In contrast, a much weaker mobility variation can be observed in junctionless devices and the threshold voltage is the principal device parameter which is dominantly affected by both electrothermal and trapping effects [21]. The observations from the pulse measurements are thus coherent with the temperature dependence observed for the JL-VNWFET devices from LAAS. Fig. 11(b) shows the I_D-V_{DS} curves under pulsed and DC conditions at -1V and -2.2V gate voltage bias for different pulse widths that exhibit this trend. The self-heating and trapping effects are expected to be activated at high gate voltages, which might explain why the difference in the drain current for different pulse widths becomes more pronounced. We can hypothesize that this phenomenon is a combined effect of both (i) trapping and (ii) electrothermal and self-heating effects. For further analyses, the VNWFET with 25 NWs with a diameter of 22 nm is selected as a representative device with the highest reproducibility and measurement stability.

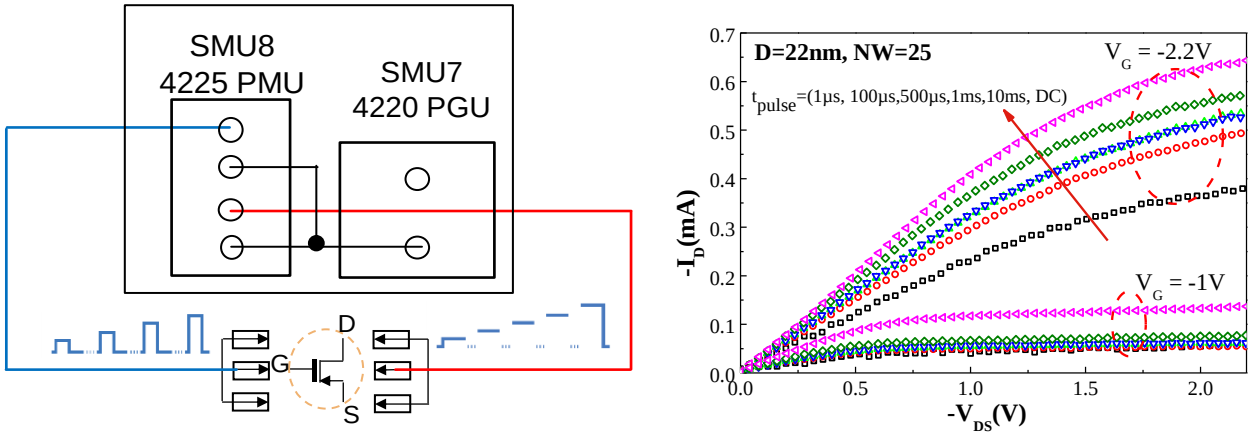

Figure 11: (a) Pulsed measurements setup; (b) I_D-V_D under DC and pulsed conditions with pulse widths varying from 1µs to 10ms at V_G=-1V and -2.2V.

II. ANALYSIS OF TRAP DYNAMICS AND ELECTROTHERMAL EFFECTS

The numerical multiphysics model developed using COMSOL (see preceding section), was leveraged for understanding of the device behavior observed under pulsed conditions. A trap-assisted model is considered to capture the effect of charge trapping in the JL-VNWFET devices. Fig. 12(a) shows the COMSOL model calibration with measurement data depicting very good model agreement. The thermal conductivity and the rise of internal temperature between the source and drain of a single nanowire for different pulse widths extracted using the COMSOL model are shown in Fig. 12(b). It can be observed that the device temperature also increases due to phonon accumulation near the drain region at high bias conditions and larger pulse widths indicating the onset of self-heating phenomena. Consequently, the temperature hot-spots are formed due to the reduction of thermal conductivity caused by phonon confinement in the 22nm nanowires. Phonon confinement can also enhance carrier trapping at the silicon-oxide interface [21]. Moreover, under higher bias, scattering mechanisms increase which have significant impact on trapping density.

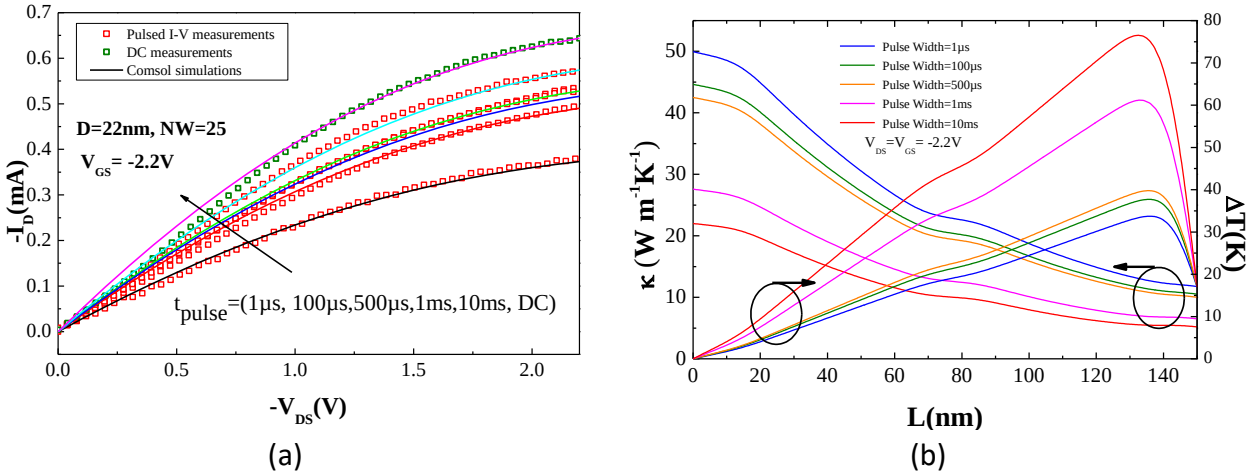

Figure 12: (a) Pulsed I_D-V_D measurements compared with compact model and COMSOL simulations; (b) Thermal conductivity and internal device temperature of the VNWFET.

Subsequently, the threshold voltage (V_{TH}) for different pulse widths are extracted for all device geometries which shows a reduction in the threshold voltage as pulse width increases as shown in

Fig. 13(a). Trapped charges at the SiO_2-Si interface, represented by the trap density N_T, alters the surface states of the nanowire leading to a modification of its surface potential and energy levels, which in turn, directly affect the V_{TH}. However, trapped charges are not the only factor that affects V_{TH}. In short channel devices, consistent with the characteristics of our VNWFET devices, the drain induced barrier lowering (DIBL) causes an additional V_{TH} drift. Due to the weak mobility variation and sensitivity of the threshold voltage to a combination of electrothermal and trapping effects, the increase in the drain current in the junctionless transistor is reflected by an equivalent temperature change inside the device (Fig. 12(b)). From the pulse measurement data for all devices under test, we extracted and compared the V_{TH} shift (Fig. 13(a)) for different pulse widths to ensure that trapping induced V_{TH} shift is equivalent in all available geometries.

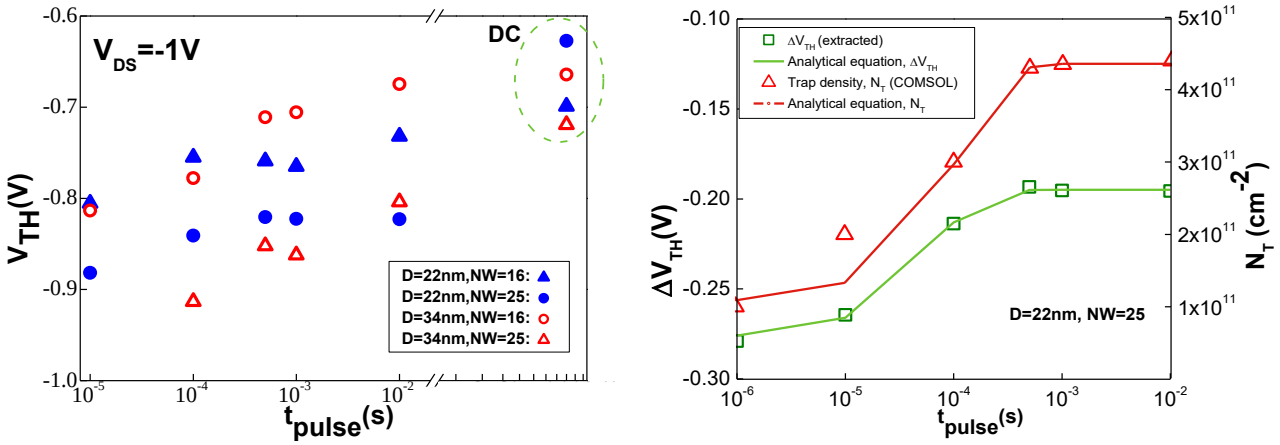

Figure 13: (a) V_{TH}-t_{pulse} for different VNWFET geometries extracted from DC and pulsed measurements; (b) ΔV_{TH}-t_{pulse}, N_T-t_{pulse} for the device with a NW diameter of 22nm and 25 NWs in parallel compared with analytical solutions.

The trap density, N_T, extracted from the COMSOL simulations, is plotted in Fig. 13 (b) (right axis) with the extracted V_{TH} shift (left axis), which show similar evolutions with pulse width. From the evolution of the V_{TH} extracted under pulsed conditions, a clear trend can be observed for all device geometries: as the pulse width continues to increase the V_{TH} values eventually saturate towards the values obtained under DC conditions. To establish a relationship between the trap density (N_T) and the observed V_{TH} drift (ΔV_{TH}), we refer to the following expression

$$\Delta V_{TH} = \frac{\alpha q N_T}{C_{OX}}, \tag{23}$$

where α is a constant, q is the electronic charge and C_{OX} is the gate oxide capacitance. From the N_T values plotted in Fig. 13(b), it can be seen that the N_T can be described by an analytical equation of the form

$$N_T = N_{SS}\left(1 - exp\left(\frac{-t_{pulse}}{\tau}\right)\right), \tag{24}$$

here N_{SS} is the maximum number of available traps, t_{pulse} is the pulse width, τ is a time constant associated with the trap activation. Using both (23) and (24), we could then plot an analytical equation ΔV_{TH} as also shown in Fig. 13(b). This affirms that the increase of the drain current with pulse width is principally governed by the trap activation that results in an equivalent shift of the device threshold voltage.

Toward modeling of electrothermal and trapping effects in JL-VNWFET

Following the extraction of thermal and trap parameters of the LAAS JL-VNWFETs, we explored implementation strategies in our previously developed VNWFET SPICE compact model [3]. This required modifying the equations describing the electrical parameters of the device that are impacted by thermal and trapping effects.

Temperature coefficients

To do so, first the temperature dependence of certain device parameters such as threshold voltage, S/D series access resistances, S/D Schottky barrier heights and intrinsic carrier concentration were defined. From the linear variation of threshold voltage versus measurement temperatures for different device geometries (different nanowires in parallel) shown in Fig. 2(b) in the experimental extraction section, an analytical model equation is obtained:

$$\Delta V_{TH} = zetaVT \times (T_{dev} - T_{nom}) \quad (25)$$

where $zetaVT$ is the slope of the curves in Fig. 2(b), T_{dev} is the internal device temperature (which is different from the measurement temperature when considering self-heating) and T_{nom} is the nominal temperature, in this case 300K, the reference measurement temperature. This analytical equation of ΔV_{TH} is then embedded in the VNWFET compact model as an additional contribution to the threshold voltage expression. Additional to this, temperature-induced variation in both access resistances and Schottky barrier height (SBH) [37] of drain and source are considered to be linear with temperature. The temperature coefficients ($zetaR, zetaPhi$) for these parameters are then introduced in the compact model in a similar manner and are integrated into the existing analytical equations for source-drain resistances ($R_{S/D}$) and Schottky barrier heights ($PhiSB_{S/D}$) as follows:

$$\Delta R_{S/D} = zetaR \times (T_{dev} - T_{nom}) \quad (26)$$

$$\Delta PhiSB_{S/D} = zetaPhi \times (T_{dev} - T_{nom}) \quad (27)$$

These new model parameters ($zetaR, zetaPhi$) are then extracted from the compact model calibration against the DC measurement data for temperature-dependent drain current.

Electrothermal network and self-heating

In addition to the drift of certain parameter values with temperature, the increase of internal device temperature (T_{dev}) during device operation is influenced by the self-heating. Under dynamic operating conditions, device thermal impedance plays an important role in governing device temperature and eventually performances at device and circuit levels. Extracted electrothermal network shown in Fig. 6 is then implemented in the compact model taking in to account the R_{TH} and C_{TH} values extracted using LF S-parameter measurements. In particular, these two parameters were used to construct an equivalent RC filter-like circuit representing the electro-thermal network [38] to account for dynamic self-heating. This required implementation of an additional fictitious node in the Verilog-A compact model that can be activated through a FLAG parameter when performing transient analysis of VNWFET logic circuits with electrothermal effects. Considering T_{sht} being the additional increase in device temperature due to self-heating, it is dynamically calculated from the voltage of the fictitious node (Fig. 14 (a)), through the following relation between its branch currents as implemented in the model,

$$P_{ssi} = \frac{T_{sht}}{R_{TH}} + C_{TH}\frac{dT_{sht}}{dt} \quad (28)$$

Here, P_{ssi} is the dissipated electrical power in Watt typically calculated by the product of drain voltage and current ($V_D \times I_D$) and the new device temperature is represented by

$$T_{dev} = T_{amb} + T_{sht} \quad (29)$$

Trapping effect

In addition to the temperature dependence of V_{TH} described by (25), eqs. (23)-(24) are used to implement an additional contribution to the threshold voltage in the compact model that reflects a V_{TH} drift with pulse width variation. This effect of charge trapping has also been implemented within the VNWFET compact Verilog-A model in a similar manner as the self-heating module, through an additional fictitious node which dynamically calculates ΔV_{TH} as the node voltage. Depending on the type of analysis another FLAG parameter was used to activate or deactivate the dynamic trapping effect in order to distinguish the trapping behavior under transient and static conditions. The implementation makes use of a similar equivalent RC filter-like circuit (Fig. 14 (b)) which recalculates the ΔV_{TH} due to trapping through the following relation:

$$\Delta \mathbf{V_{TH\_max}} = \Delta \mathbf{V_{TH}} + \boldsymbol{\tau} \frac{\boldsymbol{d\Delta V_{TH}}}{\boldsymbol{dt}}, \quad (30)$$

where ΔV_{TH_max} indicates the maximum threshold voltage shift due to trapping (signifying a saturation of trap density at large pulse widths), and τ is the trap time constant. To make the SPICE simulator interpret this dynamic trapping effect in electrical terms, the equivalent circuit is constructed with a current source ΔV_{TH_max} ($\Delta V_{TH\_max} = \alpha q N_{ss}/C_{ox}$) and two parallel R-C branches with a 1Ω resistance and a capacitance of value τ are implemented and through Kirchhoff's current rule, with the node voltage effectively representing the value of ΔV_{TH} under dynamic conditions.

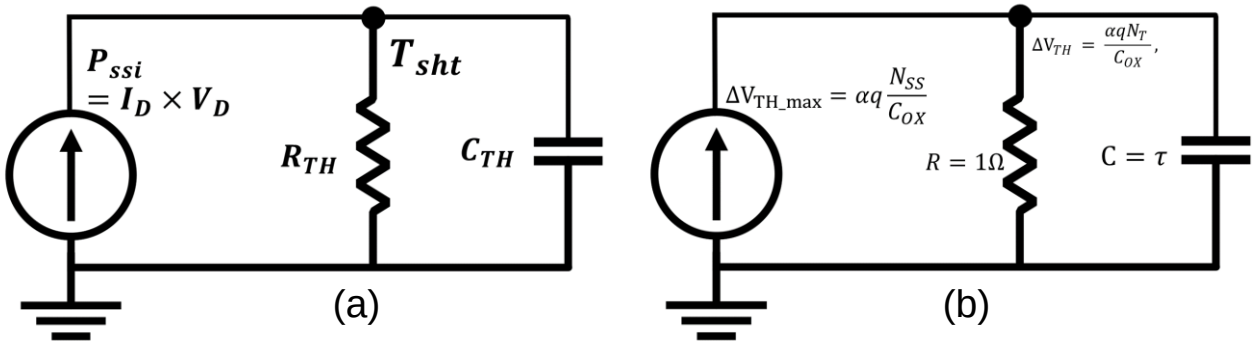

Figure 14: electrical equivalent circuit for the implementation of (a) self-heating and (b) trapping effects.

Finally, the modified compact model with the additional temperature and trap-related as well as self-heating parameters was simulated under different measurement conditions (T_{amb}) which demonstrated good model accuracy consistent with experimental results, as shown in Fig. 15.

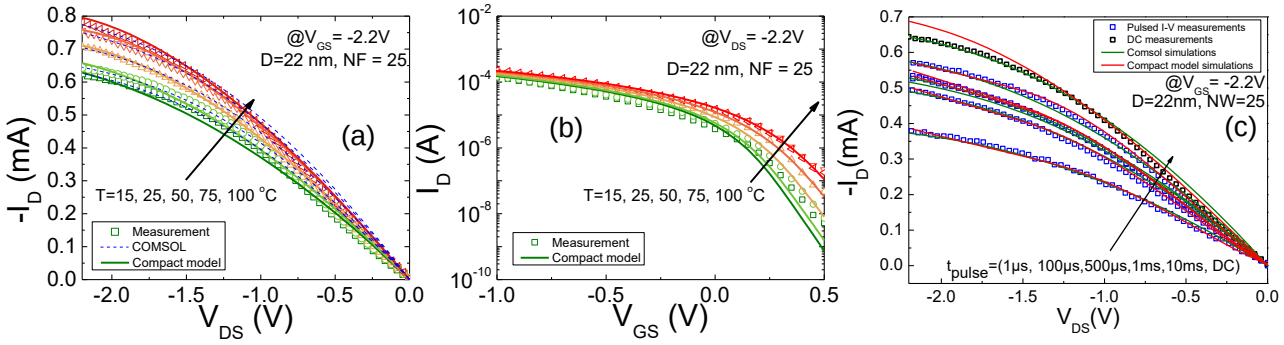

Figure 15: Evolution of drain current with (a) - (b) measurement temperatures and (c) different pulse widths, comparing experimental results, multiphysics and compact model simulations for a p-VNWFET with 25 parallel nanowires of 22 nm diameter

Conclusions

In this task, we performed a comprehensive set of on-wafer measurements of JL-VNWFETs from LAAS under a wide range of temperature and pulsed conditions to extract the thermal and trap-related parameters. In particular, DC temperature measurements and LF S-parameters were used to extract the elements of the equivalent thermal network. Pulse measurements were then used to extract trap-induced shift of the device threshold voltage. The extracted parameter values were verified through Multiphysics simulations using COMSOL. Finally, implementation methods for incorporating extracted thermal and trap parameters were explored for SPICE compact model improvement for WP3 (T2.3). The device level simulations already demonstrated very good accuracy when compared with experimental data, thus validating the accuracy of the extraction methods. In future scope of this work, the new version of the device compact model will be explored for logic circuit simulation in WP4. Additionally, transient pulse measurements and low-frequency noise characterization are planned on the new generation of the LAAS VNWFETs in order to extract complementary information on the device noise and trap related effects.

This report also demonstrates that a novel and comprehensive set of thermal and trap parameter extraction methodologies for the JL-VNWFETs are in place within the scope of WP2. For the compact modeling activities in WP3, the new version of the compact model will be crucial for the SPICE-PEX co-simulation strategy implemented by GTS. Moreover, in view of the Milestones 4 and 12 (Table 5), the extracted thermal and trap-related parameters will play an important role in accurately estimating cell-level performance for transient AC simulations and for achieving the DTCO goals. Naturally, the extracted parameter set will influence performance extrapolation at circuit level leveraging the improved compact model thus contributing directly the EDP evaluation associated with KPI4 (Table 6).

Table 5: Extract of the Schedule of relevant Milestones from DoA Annex 1 part A

Milestone number	Milestone title	WP	Lead beneficiary	Due Date (in months)	Means of verification
MS4	First set of VNWFET electrical parameters First estimation of cell performance	WP2, WP3	4 - GTS	32	PDP and EDP using measurements and compact model;

					Prediction of ultimate device dimensions using DTCO
MS12	Design-technology co-optimization flow validated	WP2, WP3	1 - UBx	44	Calculated parasitics fit experimentally extracted resistances and capacitances within a 10% error margin

Table 6: Extract of the KPI table from DoA Annex 1 part B

Key performance indicators (KPIs)	State of Art (SOA)	FVLLMONTI	OBJ
KPI4: EDP assessment for JL VNWFETs, I_{ON} of at least 300 µA/µm at a supply voltage below 0.9Vwith scaled gate length	No demonstration for scaled gate and/or p-type device	Scaled dimension and supply voltage with efficient drive current	**OBJ2** MS2 MS4

Bibliography

[1] The International Roadmap for Devices and Systems: 2022 Update.
[2] C. Maneux et al., 'Modelling of vertical and ferroelectric junctionless technology for efficient 3D neural network compute cube dedicated to embedded artificial intelligence', IEEE IEDM, San Francisco, Dec. 11-15, 2021.
[3] C. Mukherjee et al. "Compact modeling of 3D vertical junctionless gate-all-around silicon nanowire transistors towards 3D logical design," Solid-State Electron. vol. 183, p. 108125, Sep. 2021. 10.1016/j.sse.2021.108125
[4] S. Venkateswarlu, O. Badami, and K. Nayak, "Electro-Thermal performance boosting in stacked Si gate-all-around nanosheet FET with engineered source/drain contacts," *IEEE Trans. Electron Device*, vol. 68, no. 9, pp. 4723–4728, Jul. 2021.
[5] J. B. Varley et al, "Role of self-trapping in luminescence and p-type conductivity of wide-band-gap oxides," Phys. Rev. B, vol. 85, pp. 081109–04, Nov. 2012.
[6] C.-W. Lee, A. Borne, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J.-P. Colinge, "High-Temperature Performance of Silicon Junctionless MOSFETs," IEEE Transactions on Electron Devices, vol. 57, no. 3, pp. 620-625, 2010. https://doi.org/10.1109/TED.2009.2039093
[7] M. de Souza, M. A. Pavanello, R. D. Trevisoli, R. T. Doria and J. -P. Colinge, "Cryogenic Operation of Junctionless Nanowire Transistors," in IEEE Electron Device Letters, vol. 32, no. 10, pp. 1322-1324, Oct. 2011, https://doi.org/10.1109/LED.2011.2161748.
[8] B. Gentinne, J. P. Eggermont and J.-P. Colinge, "Performances of SOI CMOS OTA combining ZTC and gain-boosting techniques", Electron. Lett., vol. 32, no. 24, pp. 2092, 1995. https://doi.org/10.1049/el:19951418
[9] R. D. Trevisoli, R. T. Doria, M. de Souza, S. Das, I. Ferain and M. A. Pavanello, "The zero temperature coefficient in junctionless nanowire transistors", Appl. Phys. Lett., vol. 101, no. 6, 2012. https://doi.org/10.1063/1.4744965
[10] B. Neckel Wesling, M. Deng, C. Mukherjee, M. de Matos, A. Kumar, G. Larrieu, J. Trommer, T. Mikolajick, C. Maneux "Extraction of small−signal equivalent circuit for de−embedding of 3D vertical nanowire transistor". Solid−State Electronics, Elsevier, 2022, 194, pp. 108359. https://doi.org/10.1016/j.sse.2022.108359.
[11] P. Aminzadeh, M. Alavi, and D. Scharfetter, "Temperature dependence of substrate current and hot carrier-induced degradation at low drain bias," in VLSI Symp. Tech. Dig., 1998, pp. 178–179. https://doi.org/10.1109/VLSIT.1998.689247
[12] S. M. Sze, Physics of Semiconductor Devices, 2nd ed. New York:Wiley, 1981, p. 28.
[13] S. Grauby, E. Puyoo, M. M. Rojo, M. Martin-Gonzalez, W. Claeys and S. Dilhaire, "Effect of nanostructuration on the thermal conductivity of thermoelectric materials," 19th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), Berlin, Germany, 2013, pp. 73-78, https://doi.org/10.1109/THERMINIC.2013.6675191
[14] R. Trevisoli, R. T. Doria, M. de Souza and M. A. Pavanello, "A physically based threshold voltage definition, extraction and analytical model for junctionless nanowire transistors" Solid-State Electron. Vol. 90 pp. 12–7, 2013. https://doi.org/10.1016/j.sse.2013.02.059
[15] A. K. Sahoo, S. Fregonese, P. Scheer, D. Celi, A. Juge, and T. Zimmer, "Nonlinear modelling of dynamic self-heating in 28 nm bulk complementary metal–oxide semiconductor technology" Electron. Lett., vol. 51, pp. 581-583, 2015. https://doi.org/10.1049/el.2015.0200
[16] C. Mukherjee, M. Couret, V. Nodjiadjim, M. Riet, J. -Y. Dupuy, S. Fregonese, T. Zimmer and C. Maneux, "Scalable Modeling of Thermal Impedance in InP DHBTs Targeting Terahertz Applications," IEEE Trans. Electron Dev., vol. 66, no. 5, pp. 2125-2131, May 2019. doi: 10.1109/TED.2019.2906979

[17] N. Rinaldi, “Small-signal operation of semiconductor devices including self-heating, with application to thermal characterization and instability analysis”, IEEE Trans. Electron Devices, vol. 48, (2), pp. 323–331 2001. https://doi/org/10.1109/16.902734
[18] G. Hamaoui, N. Horny, Z. Hua, T. Zhu, J. F. Robillard, A. Fleming, H. Ban, M. Chirtoc, “Electronic contribution in heat transfer at metal-semiconductor and metal silicide-semiconductor interfaces”, Sci Rep. vol. 8, pp. 11352, 2018. https://doi.org/10.1038/s41598-018-29505-4
[19] H. Rezgui, C. Mukherjee, Y. Wang, M. Deng, A. Kumar, J. Muller, G. Larrieu, C. Maneux, “Nanoscale Thermal Transport in Vertical Gate-all-around Junction-less Nanowire Transistors- Part II: Multiphysics Simulation”, IEEE Trans. Electron Dev. 2023 (under review).
[20] A. J. Scholten, G. D.J. Smit, R.M.T. Pijper, L.F. Tiemeijer, H.P. Tuinhout, J.-L.P.J. van der Steen, A. Mercha, M. Braccioli, and D.B.M. Klaassen, "Experimental assessment of self-heating in SOI FinFETs," 2009 IEEE International Electron Devices Meeting (IEDM), Baltimore, MD, USA, 2009, pp. 1-4, https://doi.org/10.1109/IEDM.2009.5424362.
[21] Y. Wang, H. Rezgui, C. Mukherjee, M. Deng, J. Muller, S. Pelloquin, G. Larrieu, C. Maneux, “Evidence of Trapping and Electrothermal Effects in Vertical Junctionless Nanowire Transistors”, EuroSOI-ULIS, 2023.
[22] R.A. Guyer, and J.A. Krumhansl, “Thermal conductivity, second sound, and phonon hydrodynamic phenomena in nonmetallic crystals,” Phys. Rev., vol. 148, Aug. 1966. 10.1103/PhysRev.148.778
[23] A. Beardo, M. López-Suárez, L. A. Pérez, L. Sendra, M. I. Alonso, C. Melis, J. Bafaluy, J. Camacho, L. Colombo, R. Rurali, F. X. Alvarez, and J. S. Reparaz, “Observation of second sound in a rapidly varying temperature field in Ge,” Sci. Adv., vol. 7, no. 27, pp. 1–6, Jun 2021. 10.1126/sciadv.abg4677
[24] Y. Guo and M. Wang, “Phonon hydrodynamics for nanoscale heat transport at ordinary temperatures,” Phys. Rev. B, vol. 97, pp. 035421–27, Jan. 2018. 10.1103/PhysRevB.97.035421
[25] H. Rezgui, F. Nasri, M. F. Ben Aissa, and A.A. Guizani, “Investigation of nanoscale heat transport in sub-10 nm carbon nanotube field-effect transistors based on finite element method,” Therm. Sci. Eng. Prog., vol. 25, pp. 100938, Oct. 2021, 10.1016/j.tsep.2021.100938
[26] J. Lee, J. Lim, and P. Yang, “Ballistic phonon transport in holey silicon,” Nano Lett. vol. 15, pp. 3273–3279, 2015. 10.1021/acs.nanolett.5b00495
[27] A. Beardo, M. Calvo-Schwarzwälder, J. Camacho, T.G. Myers, P. Torres, L. Sendra, F.X. Alvarez, and J. Bafaluy, “Hydrodynamic heat transport in compact and holey silicon thin films,” Phys. Rev. App., vol. 11, no. 3, pp. 034003–8, Mar. 2019. 10.1103/PhysRevApplied.11.034003
[28] S. Known, M. C. Wingert, J. Zheng, J. Xiang, and R. Chen, “Thermal transport in Si and Ge nanostructure in the ‘confinement’ regime,” Nanoscale, vol. 8, no. 27, pp. 13155–13167, Jun. 2016. 10.1039/C6NR03634A
[29] A. Beardo, M. G. Hennessy, L. Sendra, J. Camacho, T.G. Myers. J. Bafaluy, and F.X. Alvarez, “Phonon hydrodynamics in frequency-domain thermoreflectance experiments,” Phys. Rev. B., vol. 101, no. 7, pp. 075303–12, Feb. 2020. 10.1103/PhysRevB.101.075303
[30] COMSOL, Inc., COMSOL Multiphysics.
[31] D. Li, Y. Wu, P. Kim, L. Shi, P. Yang, and A. Majumdar, “Thermal conductivity of individual silicon nanowires,” App. Phys. Lett., vol. 83, no. 14, pp. 2934–2936, Oct. 2003. 10.1063/1.1616981
[32] A. M. Marconnet, T. Kodama, M. Asheghi, and K. E. Goodson, “Phonon conduction in periodically porous silicon nanobridges,” Nano. Micro. Thermophys. Eng., vol. 16, pp. 199–219, Dec. 2012. 10.1080/15567265.2012.73219
[33] J. Maire, R. Anufriev, and M. Nomura, “Ballistic thermal transport in silicon nanowires,” Sci. Rep., vol. 7, p. 41794; Feb. 2017. 10.1038/srep41794

[34] A. Jain, and A. J. H. McGaughey, “Thermal transport by phonons and electrons in aluminum, silver, and gold from first principles,” Phys. Rev. B, vol. 93, pp. 081206, Feb. 2016. 10.1103/PhysRevB.93.081206
[35] H. Jiang, N. Xu, B. Chen, L. Zeng, Y. He, G. Du, X. Liu and X. Zhang, “Experimental investigation of self heating effect (SHE) in multiple-fin SOI FinFETs,” Semicond. Sci. Technol., vol. 29, no. 11, pp. 115021–7, 2014. 10.1088/0268-1242/29/11/115021
[36] B. Hai, Y. V. Tolmachev, K. A. Loparo, C. Zanelli, D. Scherson, "Cyclic versus Staircase Voltammetry in Electrocatalysis: Theoretical Aspects" J. Electrochem. Soc. vol. 158, pp. F15, 2011.
[37] S. Karataş, S. Altındal, A. Türüt, A. Özmen (2003). Temperature dependence of characteristic parameters of the H-terminated Sn/p-Si(1 0 0) Schottky contacts, 217(1-4), 250–260, 2003
[38] G. J. Coram, "How to (and how not to) write a compact model in Verilog-A," Proceedings of the 2004 IEEE International Behavioral Modeling and Simulation Conference. BMAS 2004., San Jose, CA, USA, 2004, pp. 97-106, 2004

=== End of the document ===