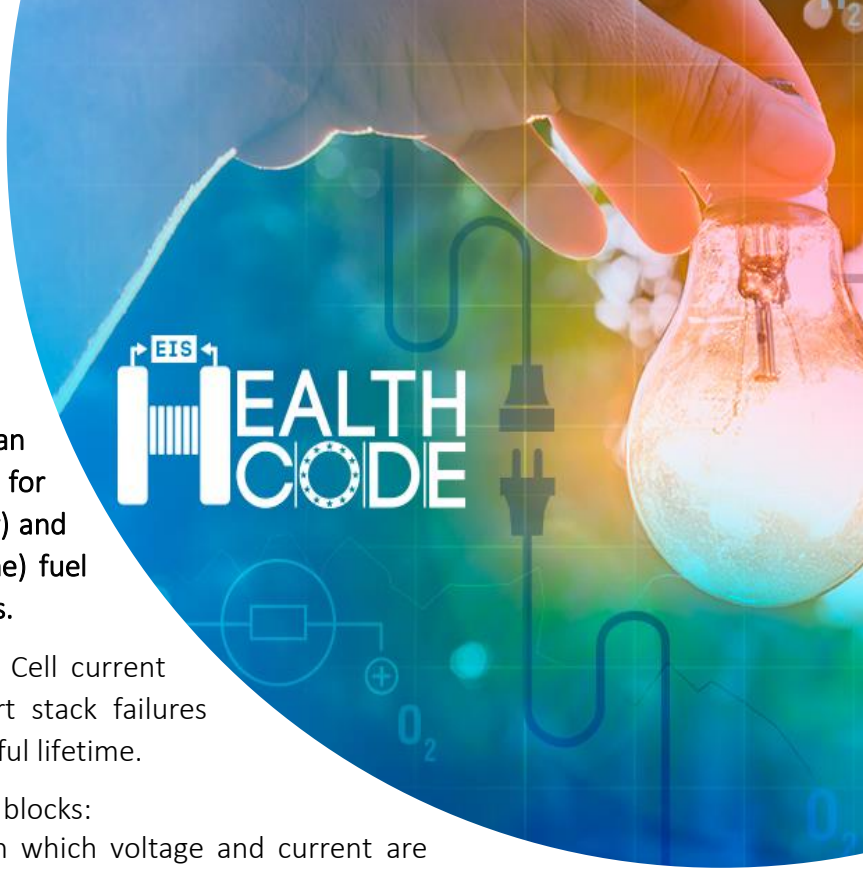
*- Public Abstract -*

# Deliverable D3.1

## 2nd Generation EIS Board Design report




**Health-Code aims at implementing an advanced monitoring and diagnostic tool for µ-CHP (Micro- Combined Heat and Power) and backup PEM (Proton Exchange Membrane) fuel cell systems equipped with different stacks.**

Such tool is able to determine the Fuel Cell current status (condition monitoring) to support stack failures detection and to infer on the residual useful lifetime.

The EIS board is composed by these main blocks:

- Analog Front End circuit, through which voltage and current are acquired (AFE)
- A new programmable device (Microcontroller unit)
- CAN bus communication, toward the DC/DC Converter.
- Serial communication ports for setting the measurement range
- Beagle Board CPU (D-CODE project legacy)

The figure below shows the block diagram of the EIS 2° generation board.

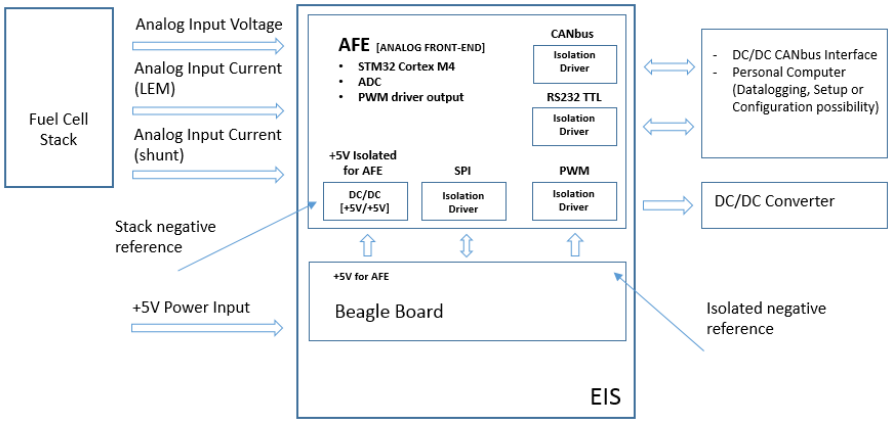



*Figure 1: EIS Board Block Diagram*

The EIS board has two intelligent and programmable devices: the first is the heart of the Beagle Board, the second is into the Analog Front End (AFE), which solves the problems discovered during the development of D-CODE and gives new space for future improvements of Health-Code performance and capability.

The RTM has been chosen to meet the important measurement limits, amplitude of the stimulation signals, period number to be acquired.

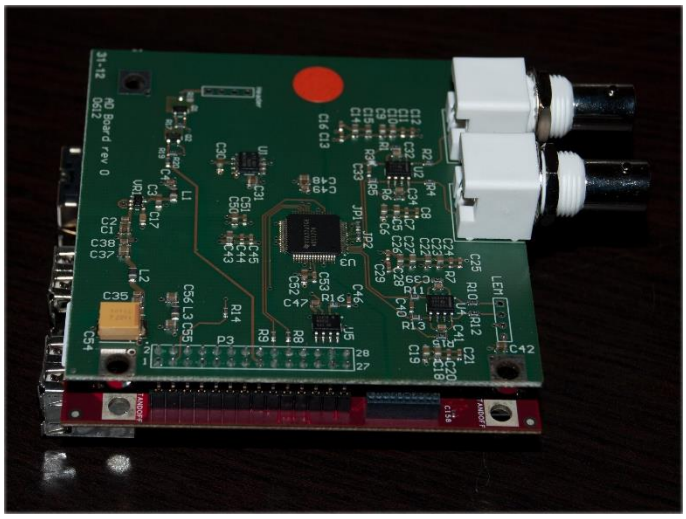


*Figure 2: EIS Board Pictorial view*

Voltage and current are sampled by the analog stage, which consists of high resolution delta-sigma (ΔΣ) analog-to-digital converters (ADCs) and by a differential amplifier circuit.
Benefits of delta-sigma (ΔΣ) Analog-to-Digital Conversion is that the filtering required to prevent aliases can be quite simple.

The communication toward DC/DC converter has been implemented in CAN open standard that is an industrial communication protocol specific for embedded systems. (CAN bus as data link layer).

EIS measurements are performed in floating mode, to have minor interference between the signal measurement made on the fuel cell stacks (Analog Front End AFE) and the FFT calculation system (Beagle Board). EIS board 2° generation has a galvanic isolation from the fuel cell stack.
The interface between CPU and RTM uses a fast (100Mbps) LAN interface. This allow the following advantages:
The Linux software can be developed and tested on a standard PC that is:
Standard sockets to manage the communication at CPU side
Linux OS to debug the RTM on AFE board
Very fast data upload to speed up the frequency analysis and to transfer data in real time.
Fast upload of the total RTM memory in 25mSec