



Neuromorphic energy-efficient secure accelerators based on phase change materials augmented silicon photonics



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This project has been funded by the Horizon Europe program under the call "CL4-2021-DIGITAL-EMERGING-01-01". It aims to create ultra-low-power, secure processors for edge computing (RIA).

AMBITIONS

- Use photonics for more energy-efficient AI technology in Europe.
- Create photonic neuromorphic accelerators that can readily integrate with RISC-V technology.
- Develop novel security layers for edge computing based on photonics.
- Demonstrate these technologies in three different industrial use-cases.
- Reduce the amount of energy needed for each operation (E/MAC) by two orders of magnitude with respect to state-of-the-art solutions for the selected use-cases.



8 countries



8 M€



15 partners



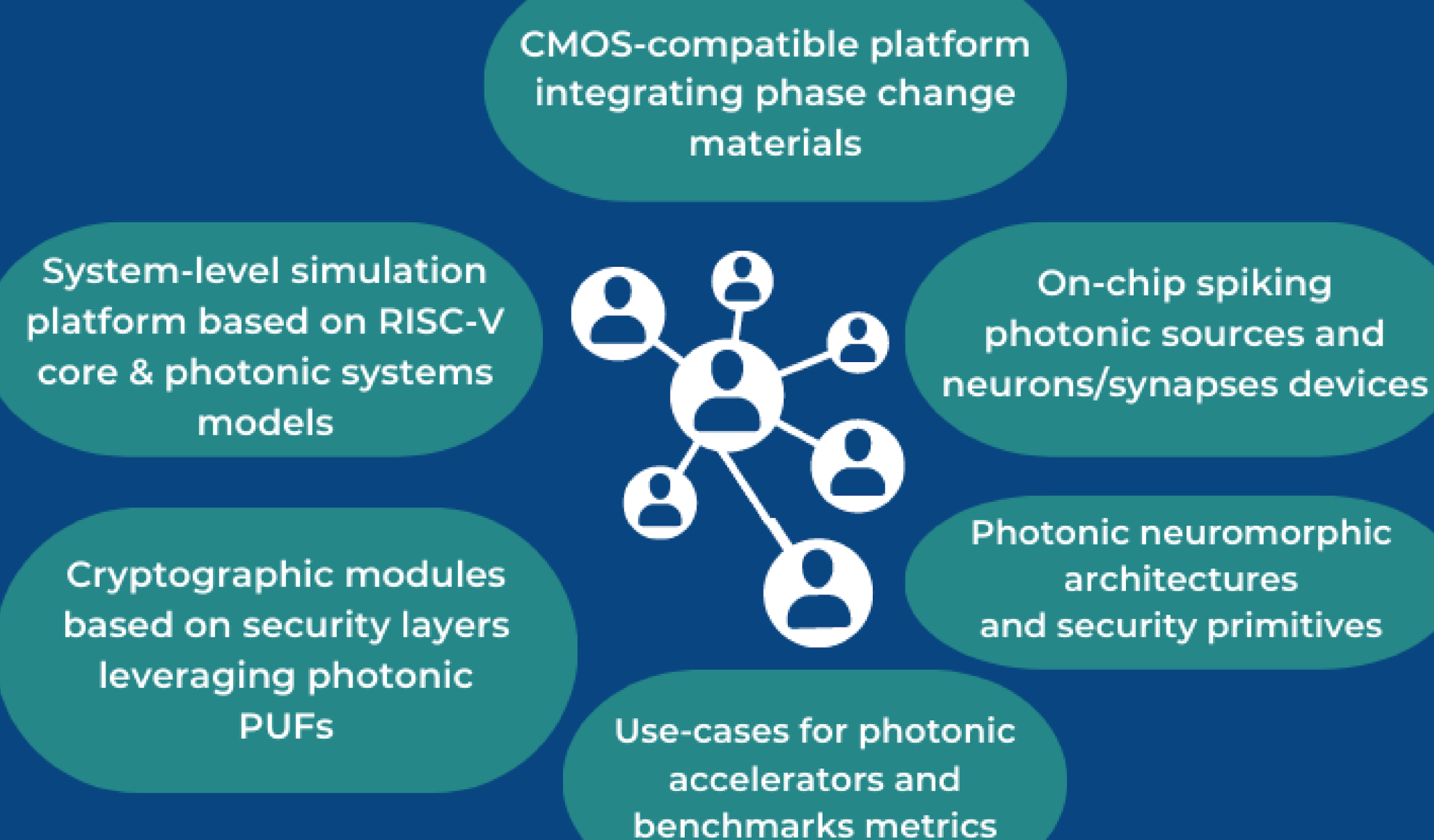
2023-2026

OBJECTIVES

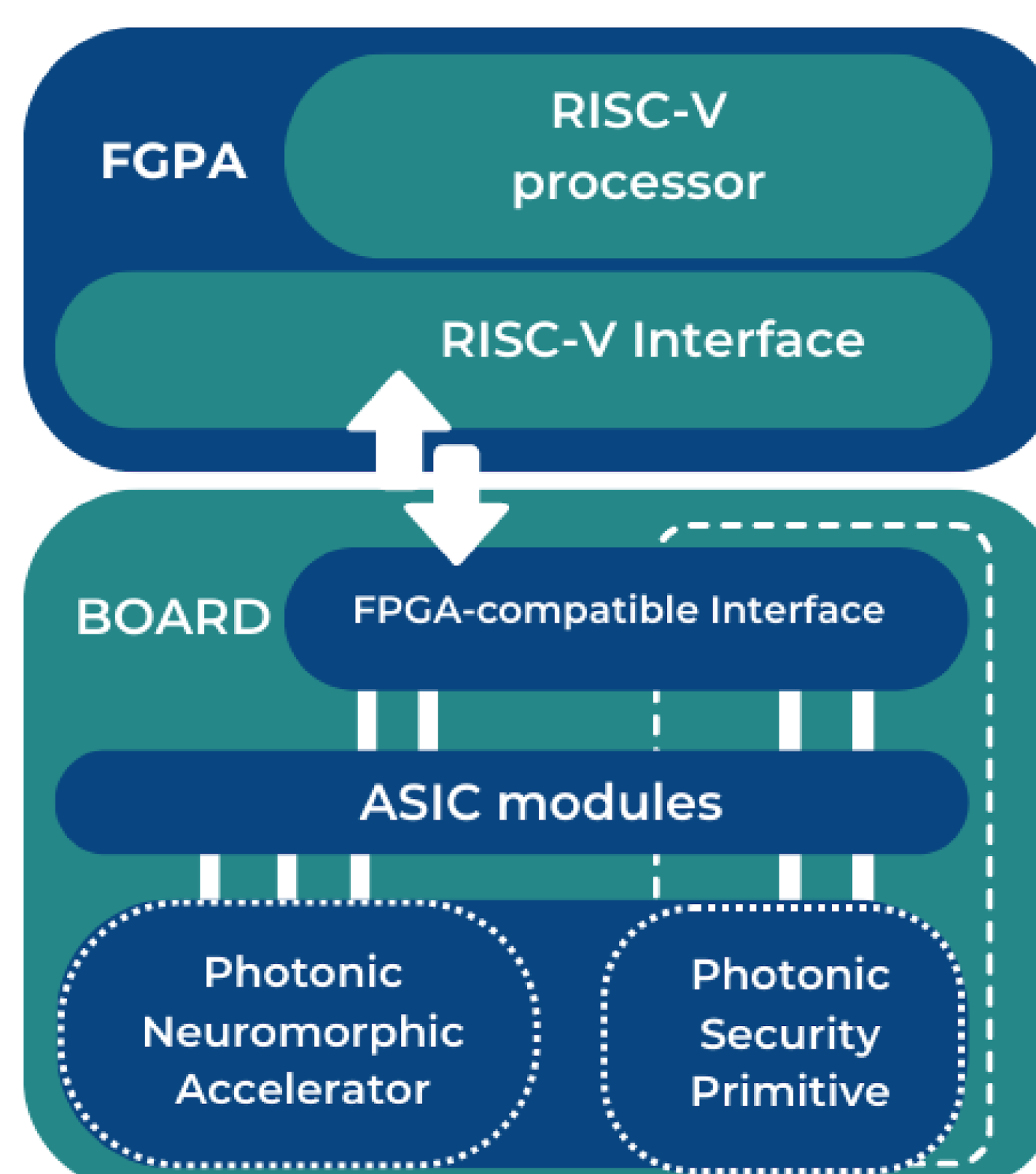
- Development of a CMOS-compatible platform addressing the integration of silicon photonics with PCMs and III-V materials.
- Development of a low-power and secure RISC-V interfaced neuromorphic accelerator based on the integration of silicon photonics, novel PCMs, and Q-switched III-V lasers.
- Development of a system-level simulation platform for PCM-based photonic low-power accelerators using photonic security layers.

CONCEPT

NOVEL CONTRIBUTIONS IN NEUROPULS



COMPUTING PLATFORM



USE CASES

- GNSS applications
- Autonomous driving
- Anomaly detection

PROPERTIES

- MAC rate ≥ 10 GHz
- Node number : 64
- Energy per MAC $< 1\text{pJ}$
- Compute density > 100 TMAC/s/mm²
- Latency < 100 ps
- Security layers

TECHNICAL APPROACH

- Develop a 300mm silicon photonics augmented platform providing novel photonic devices and architectures for next-generation energy-efficient neuromorphic accelerators.
- Develop novel lightweight photonic (light-based) neuromorphic accelerators with low latency, low energy consumption, and high operation speed for edge computing applications.
- Develop novel security primitives, i.e., physical unclonable functions, based on photonics to enhance the security strength of our RISC-V interfaced hardware computing platform.
- Develop a high-level simulation platform capable to model the behaviour of our photonic neuromorphic accelerator (and its scaling) and of its security layers.



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